DM5FXXXGXXXX

SPI-NAND FLASH

DATASHEET

Product List

Part Number	Flash Type	Capacity	Temperature	Package	Size
DM5F001GUPIY	SLC	1Gbit	-40℃ ~ 85℃	LGA-8	6x8mm
DM5F002GUPIY	SLC	2Gbit	-40℃ ~ 85℃	LGA-8	6x8mm
DM5F004GUPIY	SLC	4Gbit	-40℃ ~ 85℃	LGA-8	6x8mm

Rev1.7 2025

Damay semi

SHENZHEN DAMAY SEMICONDUCTOR COMPANY LIMITED

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1. Description

The DM5FXXXGXXXX is a SPI NAND Flash , With Built-in Controller supports the high-speed NAND interface, including ONFI 2.x and Toggle mode, to achieve the maximum datatransfer rate for ever higher performance.

2. Features

- ECC
  - BCH 70/65/40/24/16/8 (Data unit: 1KB)

- Standard, Dual and Quad SPI
  - Standard: SCLK, CS, SI, SO, WP, HOLD
  - Dual: SCLK, CS, SIO0, SIO1, WP, HOLD
  - Quad: SCLK, CS, SIO0, SIO1, SIO2, SIO3
  - Clock frequency: 104MHz (maximum)

- Enhanced access performance
  - 4KB cache for fast random read
  - Cache read and cache program

- Software/Hardware write protection
  - Write protect all/option of memory via software
  - Enable/Disable protection with WP pin

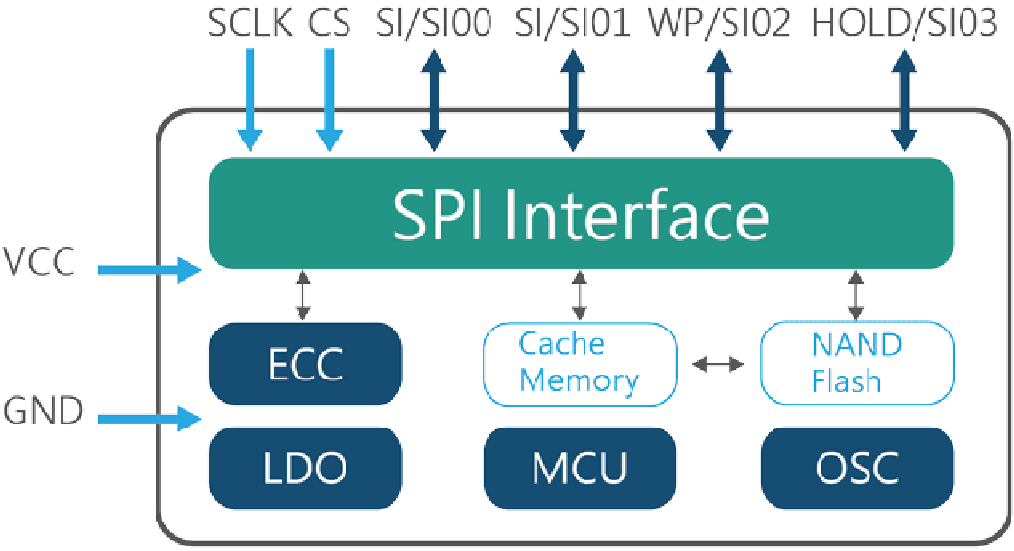
- Security
  - 8 pages for OTP region

- Others
  - Support Data Randomizer

  - Support Wear Leveling
  - Support Bad block management
  - Support Program Fail Recovery
  - Automatic power saving operation

- Temperature
  - Operation : Industrial:-40^{O}C ~ 85^{O}C
  - Storage: -55^{O}C ~ 125^{O}C

3. Block Architecture



4. Product List

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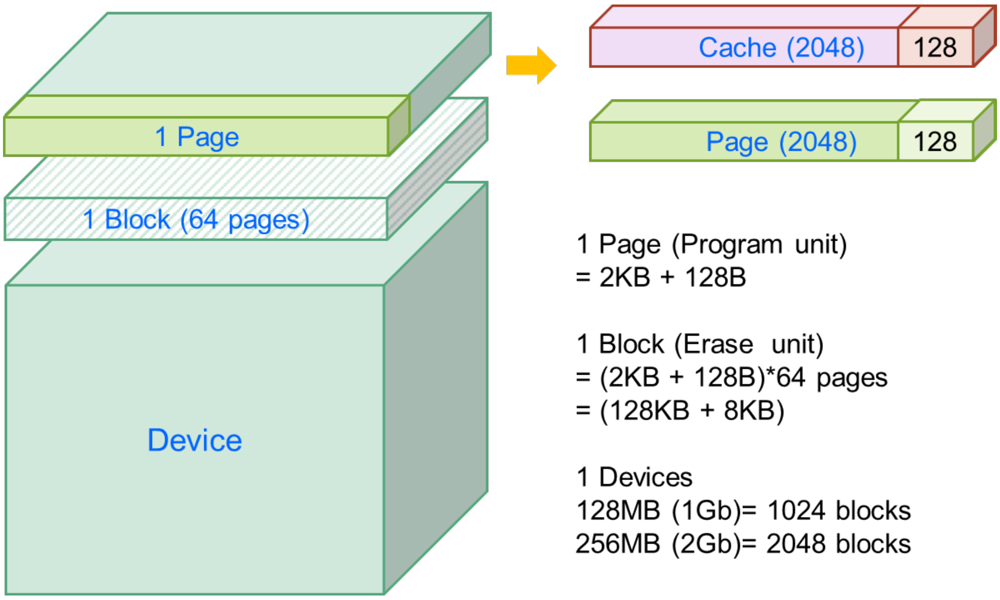
DM5F001GUPIY	SLC	1Gbit	-40°C ~ 85°C	LGA-8	6x8mm
DM5F002GUPIY	SLC	2Gbit	-40°C ~ 85°C	LGA-8	6x8mm
DM5F004GUPIY	SLC	4Gbit	-40°C ~ 85°C	LGA-8	6x8mm

5. Flash Organization

Example: if 1Page=

2KB+128B



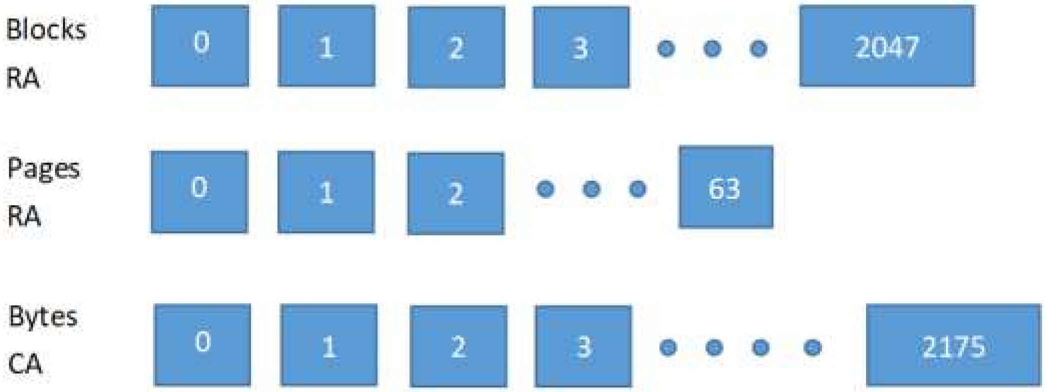
1 Page (Program unit)
= 2KB + 128B

1 Block (Erase unit)
= (2KB + 128B)*64 pages
= (128KB + 8KB)

1 Devices
128MB (1Gb)= 1024 blocks
256MB (2Gb)= 2048 blocks

6. Memory Address MAP

Hereunder is a sample.



Note:

1. RA: Row address is used for addressing the page or block location
   RA[5:0]: for page range 0 ~ 63
   RA[16:6]: for block rage 0 ~ 2047
2. CA: Column address is used for addressing the Byte location. The CA has the range 0~2175.

7. FTL Engine

DM5FXXXGXXXX have the FTL engine to provide more advance features.

Hereunder is the additional highlight items for application.

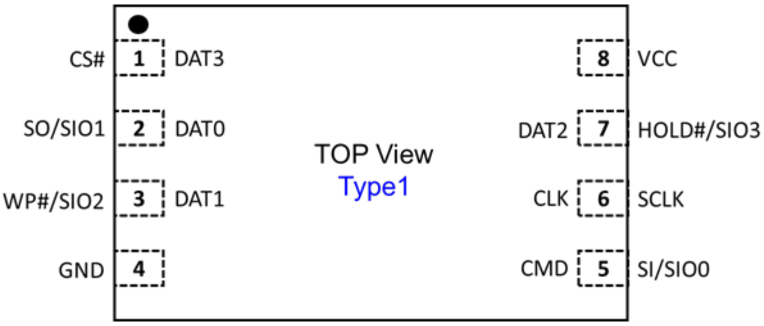
1. DM5FXXXGXXXX provide several important features
   A. Randomizer: DM5FXXXGXXXX has the randomizer to convert the data into the average distribution of zero and one in advance to solve the chance of misjudgment of data.
   B. FTL : DM5FXXXGXXXX has FTL to do wear Leveling and can do bad block management,

2. Reserve 10 blocks for FTL engine
3. Spare area: DM5FXXXGXXXX for the maximum ECC , so customer can not use the spare area.

8. Package Description

LGA8

Device Top View



Pin Definition

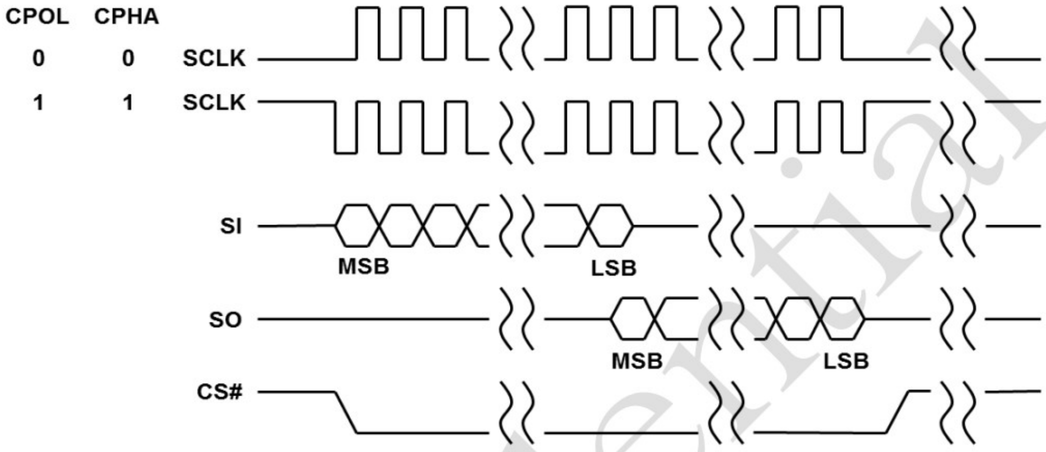
Pin Name	IO type	Description
CS#	Input	SPI chip select
SO/SIO1	In/Out	SPI output (one bit mode) SPI D1 (Quad mode)
WP#/SIO2	In/Out	SPI write protect (one bit mode) SPI D2 (Quad mode)
GND	Ground	Ground pin
SI/SIO0	In/Out	SPI input (one bit mode) SPI D0 (Quad mode)
SCLK	Input	SPI clock
HOLD#/SIO3	In/Out	SPI hold (one bit mode) SPI D3 (Quad mode)
VCC	Supply	Main supply power

9. SPI Protocol

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCLK and output data is available on the falling edge of SCLK for both mode 0 and mode 3. The timing diagrams show in this data sheet are mode 0.



SCLK	SCLK provides interface timing for SPI NAND. Address, data and commands are latched on the rising edge of SCLK. Data is placed on SO at the falling edge of SCLK.
CS#	When CS# = 0, the device is placed in active mode. When CS# = 1, the device is placed in inactive mode and SO is High-Z.

Standard SPI (one bit mode):

Standard serial peripheral interface on four signals bus: System Clock (SCLK), Chip Select (CS#), Serial Data In (SI) and Serial Data Out(SO).

Dual SPI:

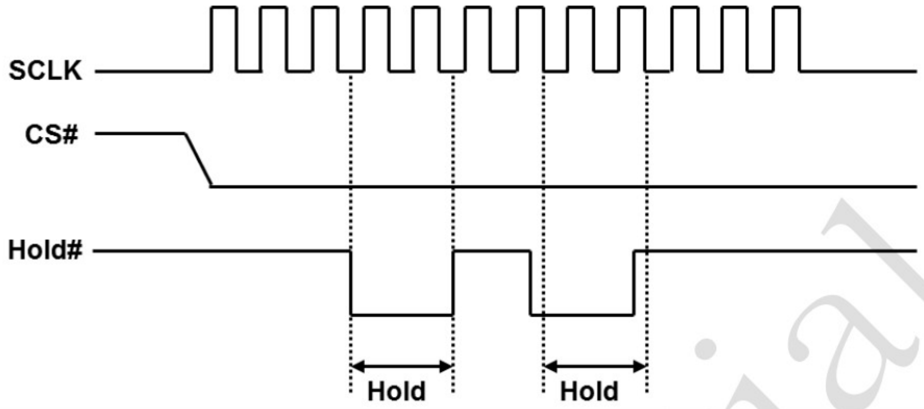
SPI operate in this mode can work with x2 data bus width for data. These commands allow data to be transferred to or from SPI at the 2x speed than standard SPI. The SI and SO become bi-directional I/O pins: SIO0 and SIO1.

Quad SPI:

In this mode the HOLD# and WP# signal become two additional data access pin and make SPI is allowable to transfer 4x data than standard mode can. There will be total 4 data pin in this mode, SI for SIO0, SO for SIO1, WP# for SIO2, HOLD# for SIO3 and all bi-directional as well.

Hold Mode:

The HOLD # signal goes low to stop any serial communications with the device, but doesn't stop the operation of write status register, programming or erasing in progress.



HOLD	Hold mode starts at the falling edge of HOLD# provided SCLK is also LOW. If SCLK is HIGH when HOLD# goes LOW, hold mode begins after the next falling edge of SCLK.

Write Protection Mode:

Write protect (WP#) provides hardware protection mode. The WP# prevents the block lock bits (BP0, BP1, and BP2) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits can't be altered.

10. Command List

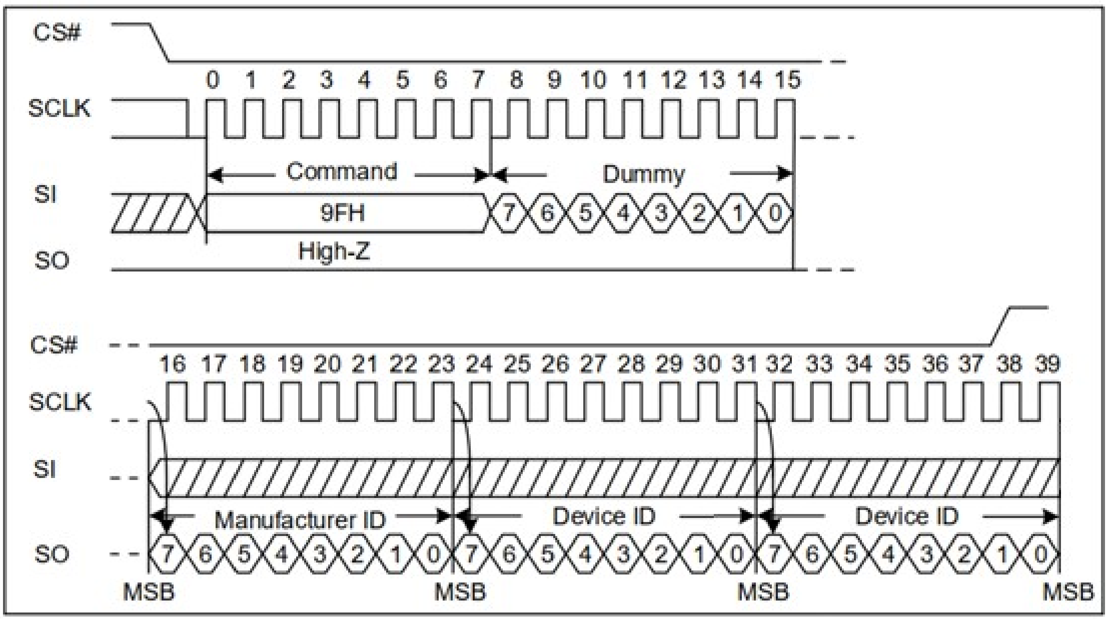
Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte N
Write Enable	06H					
Write Disable	04H					
Get Features	0FH	A7-A0	(D7-D0)			
Set Feature	1FH	A7-A0	(D7-D0)			
Page Read (to cache)	13H	A23-A16	A15-A8	A7-A0		
Fast Read from Cache	03H/0BH	A15-A8	A7-A0	dummy	(D7-D0)	
Read from Cache x2	3BH	A15-A8	A7-A0	dummy	(D7-D0)/2	
Read from Cache x4	6BH	A15-A8	A7-A0	dummy	(D7-D0)/4	
Read from Cache Dual IO	BBH	A15-A8/2	A7-A0/2	Dummy/2	(D7-D0)/2	
Read from Cache Quad IO	EBH(3)	A15-A8/4	A7-A0/4	Dummy/4	Dummy/4	(D7-D0)/4
Read ID	9FH	dummy	(MID)	(DID)	(DID)	
Program Load	02H	A15-A8	A7-A0	(D7-D0)	Next Byte	Byte N
Program Load x4	32H	A15-A8	A7-A0	(D7-D0)/4	Next Byte/4	Byte N/4
Program Execute	10H	A23-A16	A15-A8	A7-A0		
Program Load Random Data	84H(2)	A15-A8	A7-A0	(D7-D0)	Next Byte	Byte N
Program Load Random Data x4	C4H/34H	A15-A8	A7-A0	(D7-D0)/4	Next Byte/4	Byte N/4
Program Load Random Quad IO	72H(2)(3)	A15-A8/4	A7-A0/4	(D7-D0)/4	Next Byte/4	Byte N/4
Block Erase	D8H	A23-A16	A15-A8	A7-A0		
Reset	FFH					

Note:

1. Dummy pattern is all byte unit instead of clock cycles. For example. Dummy pattern in one bit mode is 1 byte 8 clock cycles and in dual mode is 1 byte 4 clock cycles, 1 byte 2 clock cycles in quad mode.
2. These commands are for internal data move only.
3. The QE bit needs to be set while these commands are about to be executed.
4. Dual SPI Address Input (**CA15-8 / 2** and **CA7-0 / 2**) format:
   IO0 = x, x, CA10, CA8, CA6, CA4, CA2, CA0
   IO1 = x, x, CA11, CA9, CA7, CA5, CA3, CA1
5. Dual SPI Data Output (***D7-0 / 2***) format:
   IO0 = D6, D4, D2, D0, ……
   IO1 = D7, D5, D3, D1, ……
6. Quad SPI Address Input (**CA15-8 / 4** and **CA7-0 / 4**) format:
   IO0 = x, CA8, CA4, CA0
   IO1 = x, CA9, CA5, CA1
   IO2 = x, CA10, CA6, CA2
   IO3 = x, CA11, CA7, CA3
7. Quad SPI Data Input/Output (***D7-0 / 4***) format:
   IO0 = D4, D0, …… IO1 = D5, D1, ……
   IO2 = D6, D2, …… IO3 = D7, D3, ……

11. Read ID (9FH)

Read ID command is used for identifying the part category of SPI NAND. User could use this command to check if the ID match their application.



MID	A1

DID1	SPI	SD
	0F	0D

DID2	1Gb	2Gb	4Gb	8Gb	16Gb	32Gb	64Gb	128Gb	256Gb	512Gb
	01	02	03	04	05	06	07	08	09	10

12. Write Enable/Disable

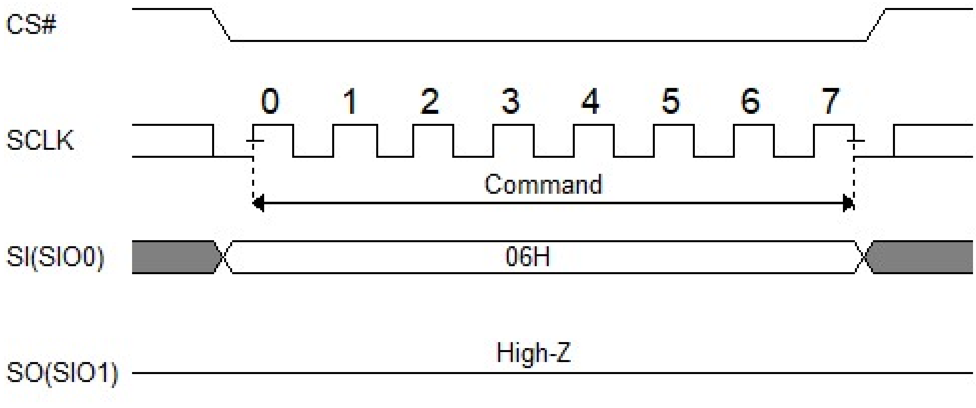
12.1. Write Enable (06H)

Before starting to program a SPI FLASH, the WRITE Enable should be executed. It's to protect the SPI NAND from leakage and some unknown damage.

Write Enable is issued priori to following command

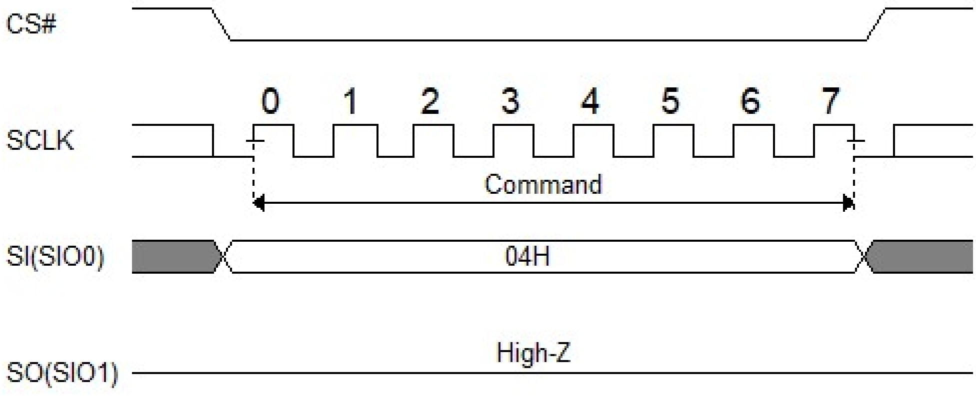
- Page program
- OTP program/OTP protection
- Block erase

The Write enable will be cleared after a reset command.



12.2. Write Disable (04H)

To reset the "Write enable" command user can issue the Write Disable.



13.SPI NAND Features

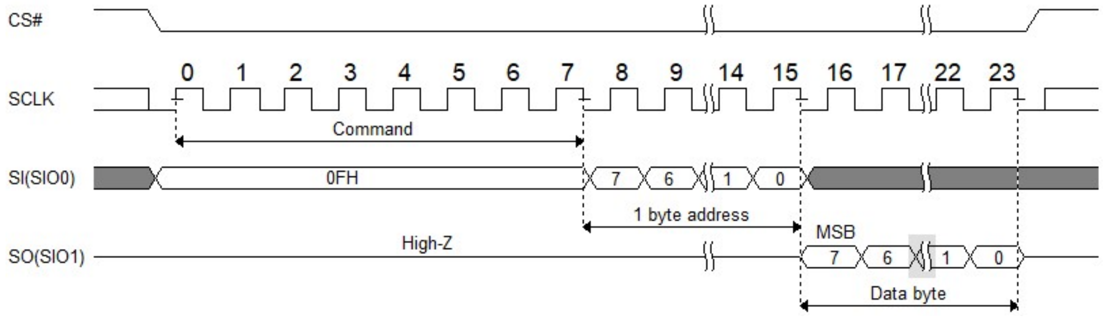
In order to access the SPI NAND features, Get Feature (0FH) and Set Feature (1FH) are used. These commands are used to monitor the device status and change the device behavior. These commands use a one byte feature address to determine which feature is to be changed or read.

The supported feature is list in following

Register	**Addr**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Protection	A0H	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Featured	B0H	OTP_PRT	OTP_EN	Reserved	Reserved	Reserved	Reserved	Reserved	QE
Status	C0H	Reserved	ECCS2	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Strength	D0H	Reserved	DS_S1	DS_S0	Reserved	Reserved	Reserved	Reserved	Reserved

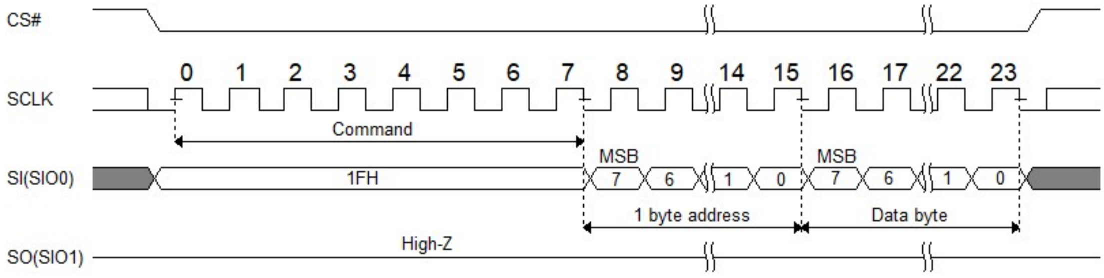
13.1. Get Feature (0FH)

Get feature (0FH) are following by one byte data to monitor the status of the internal register.



13.2. Set Features (1FH)

Set feature (1FH) issue one byte registered data to control the internal register of SPI NAND.



14. READ

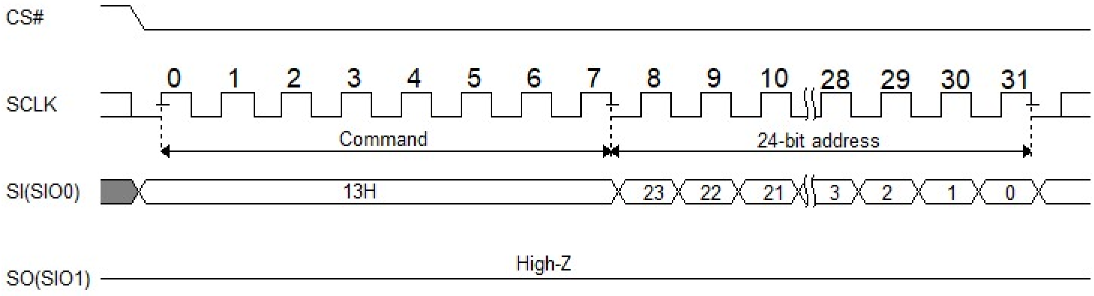
Read commands are used for retrieving data for SPI. User can issue following command to require data in different way according to the application scenario.

- 13H (PAGE READ to cache)
- 0FH (GET FEATURES command to read status)
- 03H or 0BH (Read from cache)/3BH (Read from cache x2)/6BH (Read from cache x4)/BBH (Read from cache dual IO)/EBH (Read from cache quad IO)

The page address has 24-bit width to allocate desired address. After the block/page addressing are done, the device starts the transfer from the main array to the cache register and is busy for tRD time. During this time, the GET FEATURE (0FH) command can be issued to monitor the status. When page read command is done the RANDOM DATA READ commands can be followed to read out desired data from cache. Once the maximum byte of a page is reached the following output data will wrap around until the CS# is released to high.

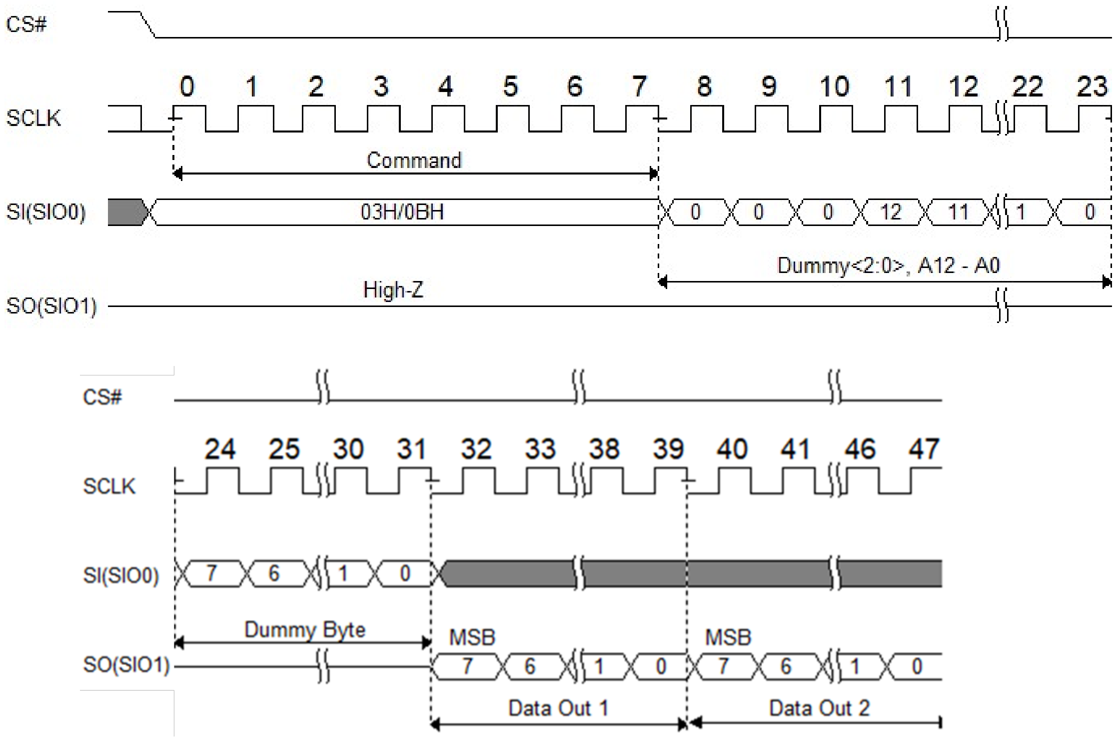
14.1. Read to Cache(13H)

Read to cache are mainly used for moving the data inside NAND FLASH to the cache memory of controller. While user issue this command controller translate the address to the NAND address and issue the NAND interface to locate user data. Once the data is located it will be transferred from the NAND to the controller cache.



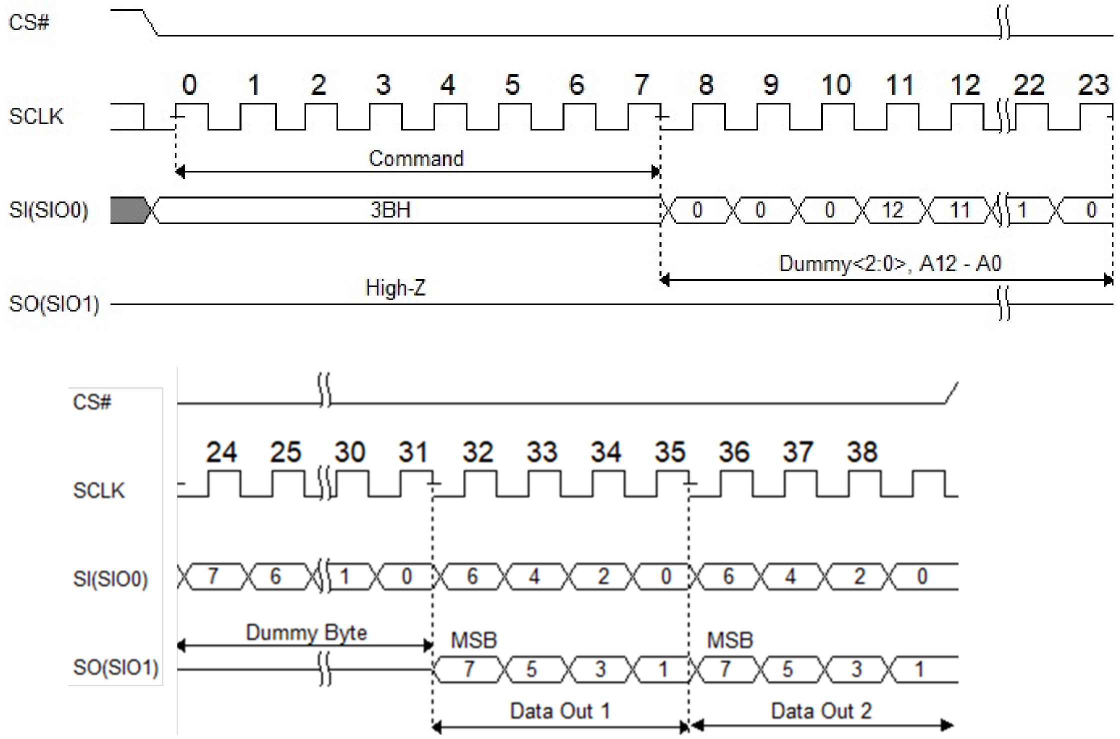
14.2. Read from Cache (03H or 0BH)

The cache in the SPI NAND can be seen as a buffer to access. User can use the cache to store or retrieve data. Once the data was read in the cache (user should take care of it) the command of Read from Cache can be used to get the cache data through the SPI interface. It’s recommended to get cache data by word-align way to prevent unpredictable situation. Cache will be empty during sleep mode.



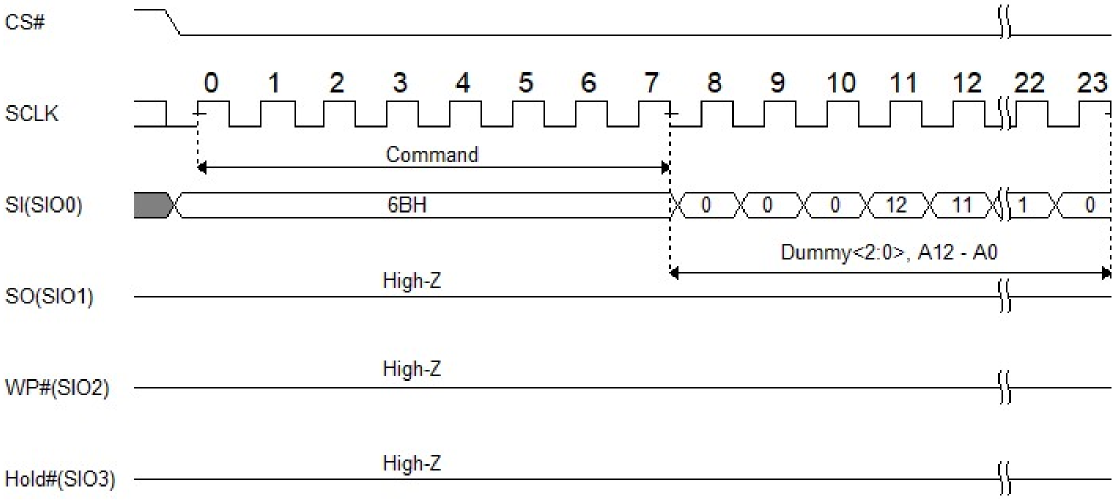
14.3. Read from Cache x2 (3BH)

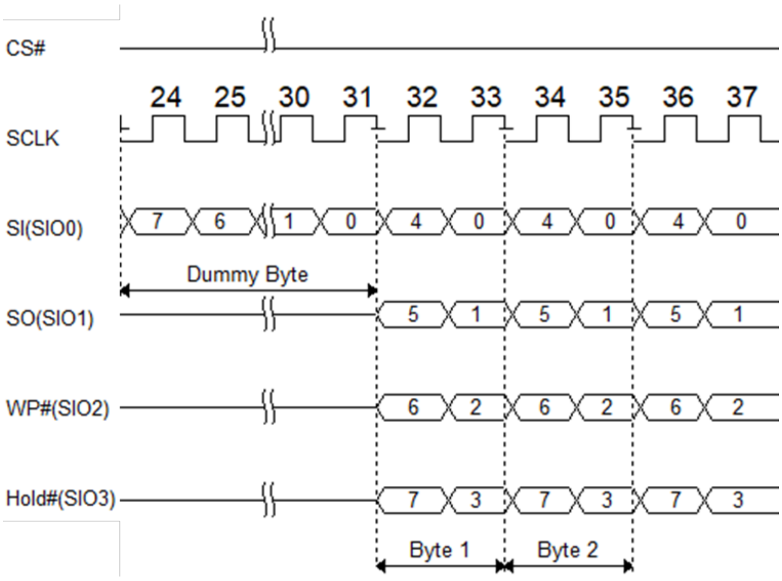
In order to enhance the bus efficiency SPI NAND offers a way to access cache with 2x bus width. In this mode SI and SO stands for SIO0 and SIO1 which mean the data can be either input or output in these two pins. Therefore, the data rate will be twice than the one bit mode.



14.4. Read from Cache x4 (6BH)

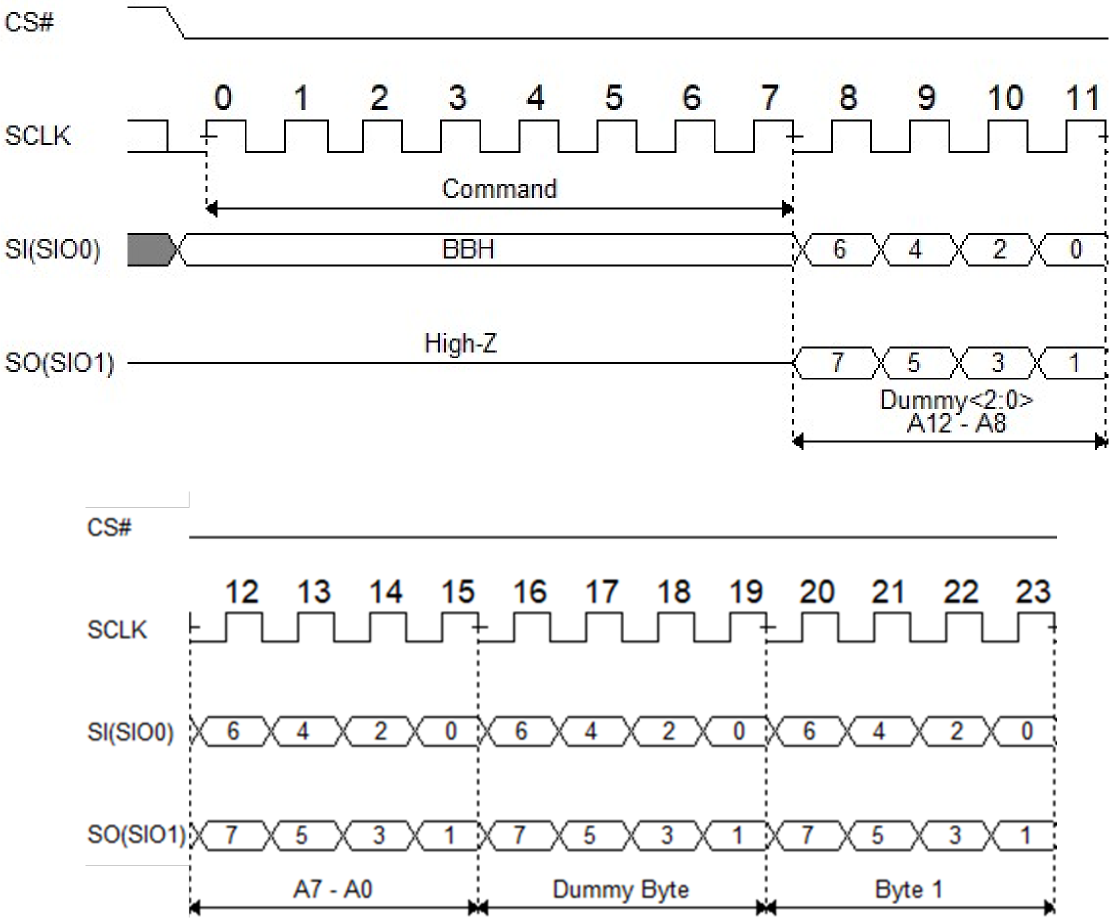
The ultimate way to access a SPI NAND is to use all the data pin. For maximizing the utilization of the data pin, the SPI NAND can access the data from cache to all its pin. In other word, it increases the data rate with 4 times. In order to implement this feature, WP# and HOLD# pin are adopted as part the data pin, and the HOLD and WP feature will be neglected temporarily.





14.5. Read from Cache Dual IO (BBH)

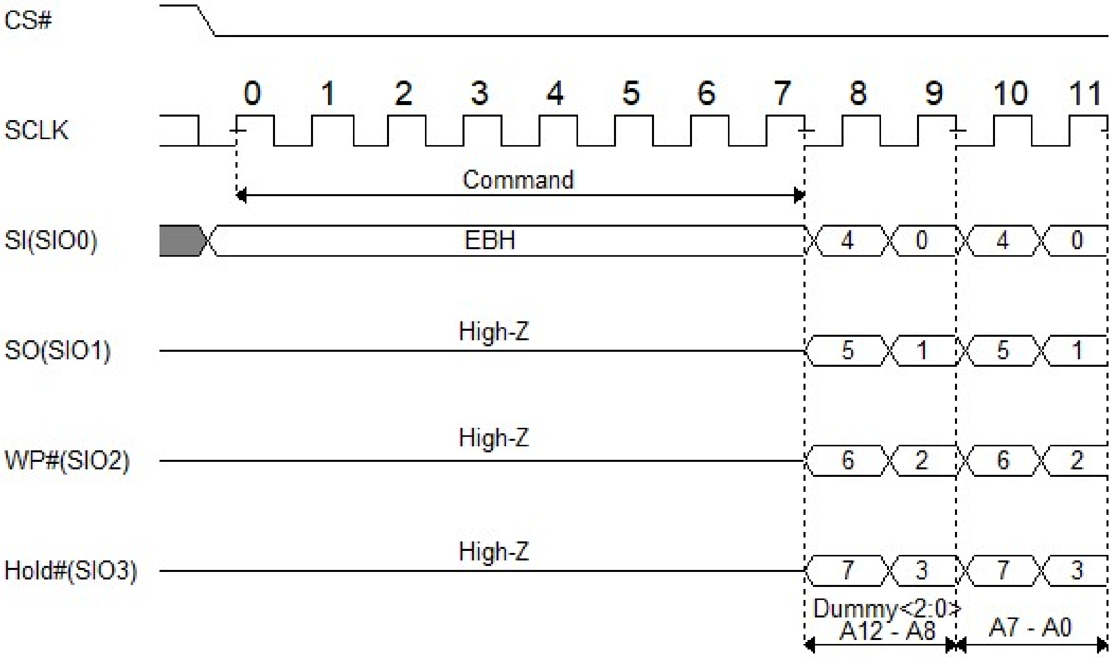
In order to maximize the bus efficacy more over. The commands are seen as the address in dual IO mode. Therefore, the dual IO mode can issue address in SIO0 and SIO1 as following.

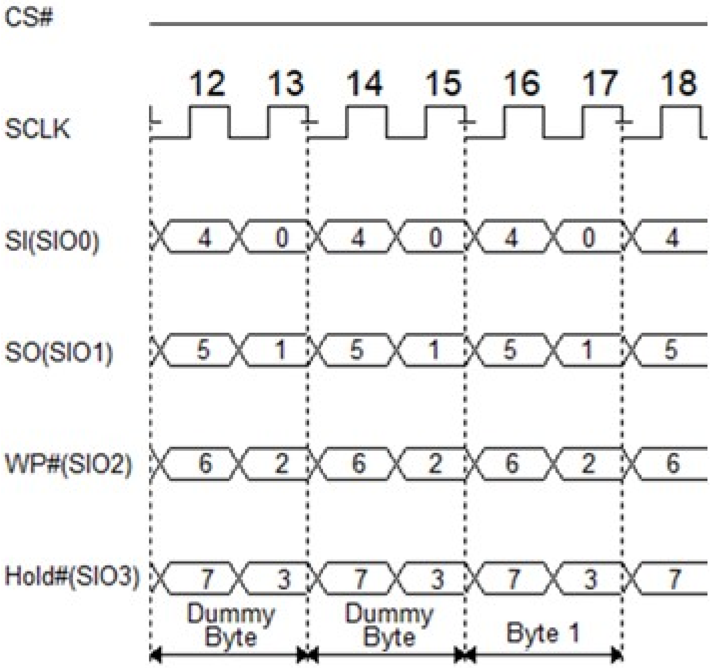


Please be noticed, the dummy byte is four clock cycles here.

14.6. Read from Cache Quad IO (EBH)

As in the dual IO mode, quad IO mode can expend the address to four data pin to extend the bus advance.





Please be noticed, the dummy byte is two clock cycles here.

15. PROGRAM

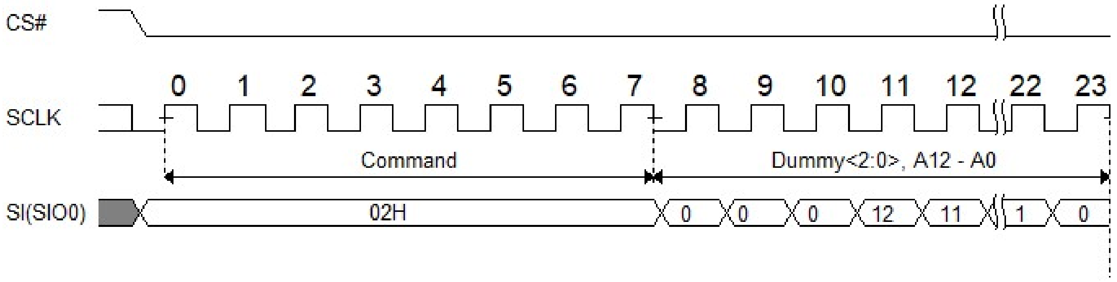
The program command is intended to write data into SPI NAND. Due to there is a cache as a buffer between the SPI interface and NAND FLASH the program command are separated to loading and executing command. The program sequence can be categorized into two flows as following.

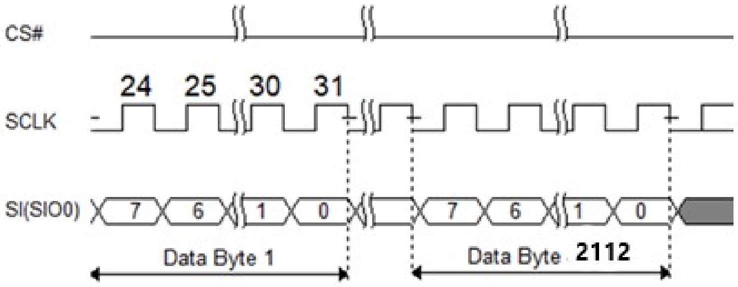
- 06H (WRITE ENABLE)
- 02H (PROGRAM LOAD)/32H (PROGRAM LOAD x4)
- 10H (PROGRAM EXECUTE)
- 0FH (GET FETURE command to read the status)

The first command of program is PROGRAM LOAD (02H/32H) command. It consists of an 8-bit command and following by 3 dummy bits and 13-bit column address then data bytes. The data bytes are loaded into a cache register to the limitation of cache size. Data over cache size will be neglected. The command sequence ends when CS# goes from LOW to HIGH. Then prior to performing the PROGRAM EXECUTE operation, a WRITE ENABLE (06H) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued. Then the rest of the program sequence is ignored.

15.1. Program Load (02H)

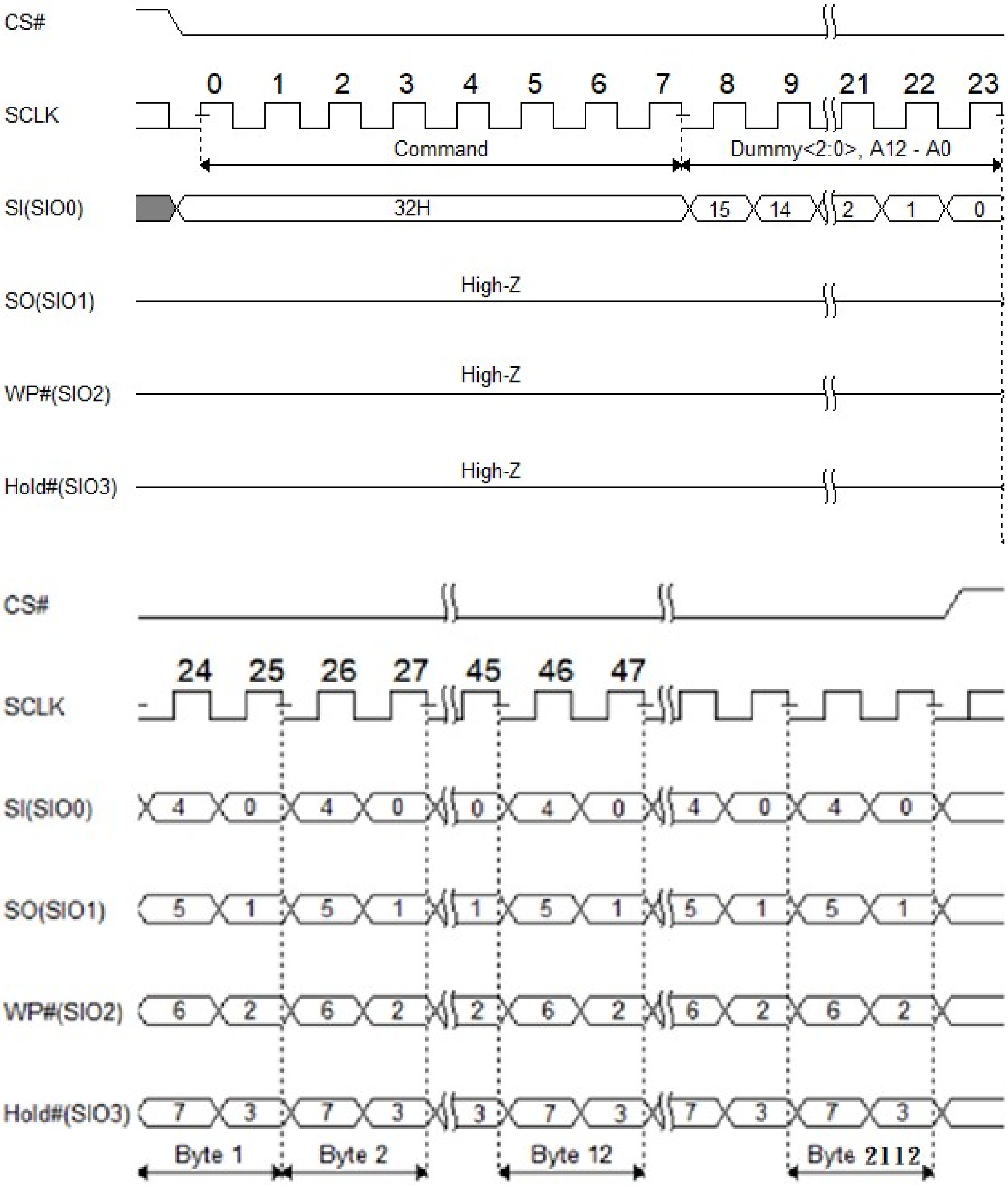
Program load command enable user to transfer data from the SPI interface to the controller. The data will be put in controller until user issue the program execute.





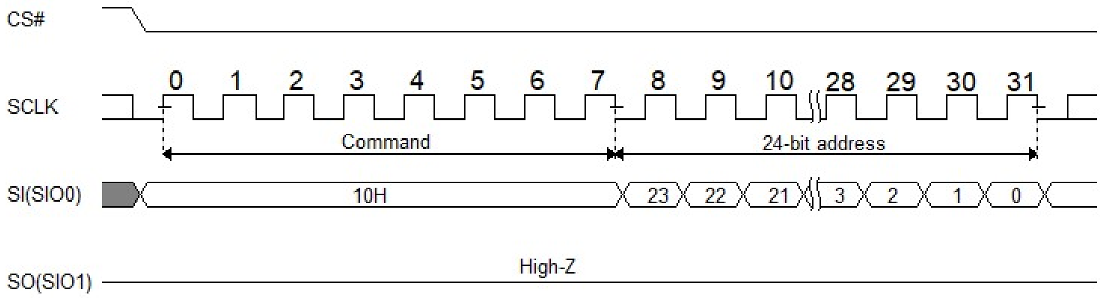
15.2. Program Load x4 (32H)

In this mode data is transferred in four data pin and the data rate could be increase accordingly. Before use this mode the QE bit should be set to high in advance.



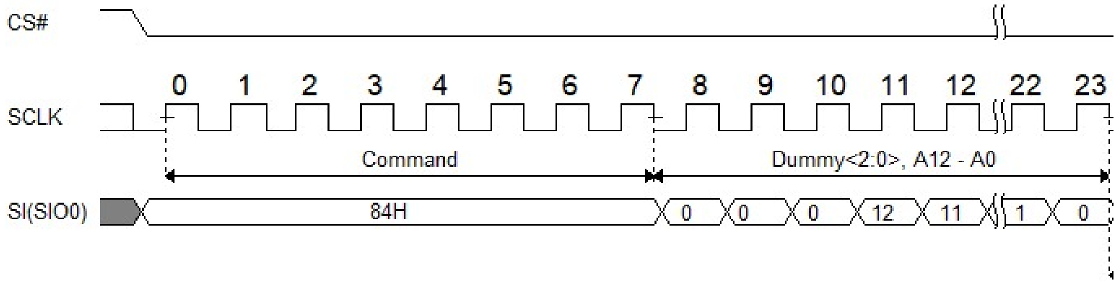
15.3. Program Execute (10H)

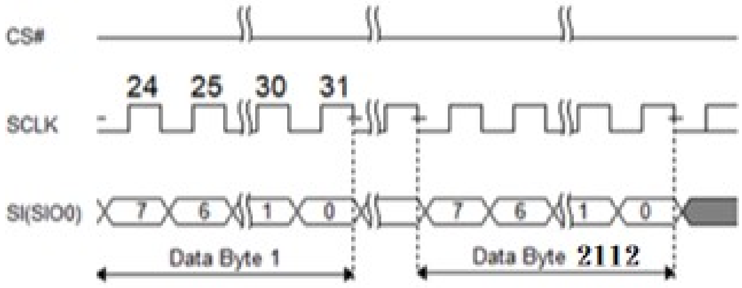
While user issue the program execute the controller start to execute FLASH program command to a NAND FLASH. The program time last a while and it depends on the parameter, tPROG. During the Program busy time user can keep monitoring the status to check if the program is finished. Next program load command won’t be able to issue until the program execute is done.



15.4. Program Load Random Data Move (84H)

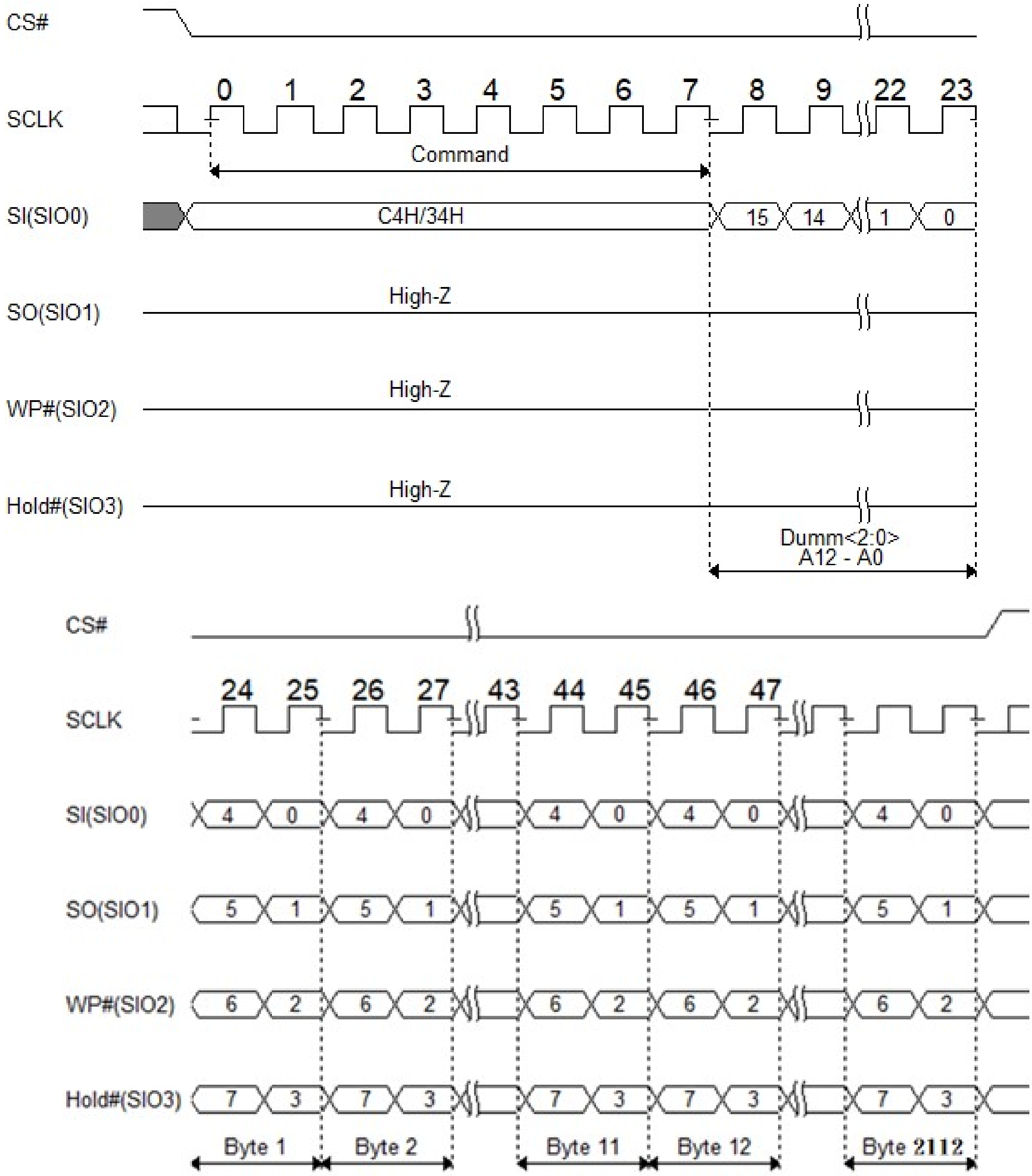
The SPI NAND cache can be seen as a buffer, so user can move the data in or out according to the address. The internal data move is used for attaching or removing data inside a page. The operating address should within a page size. Despite the freedom of using internal data move please access in word-align manner to prevent unpredictable situation.





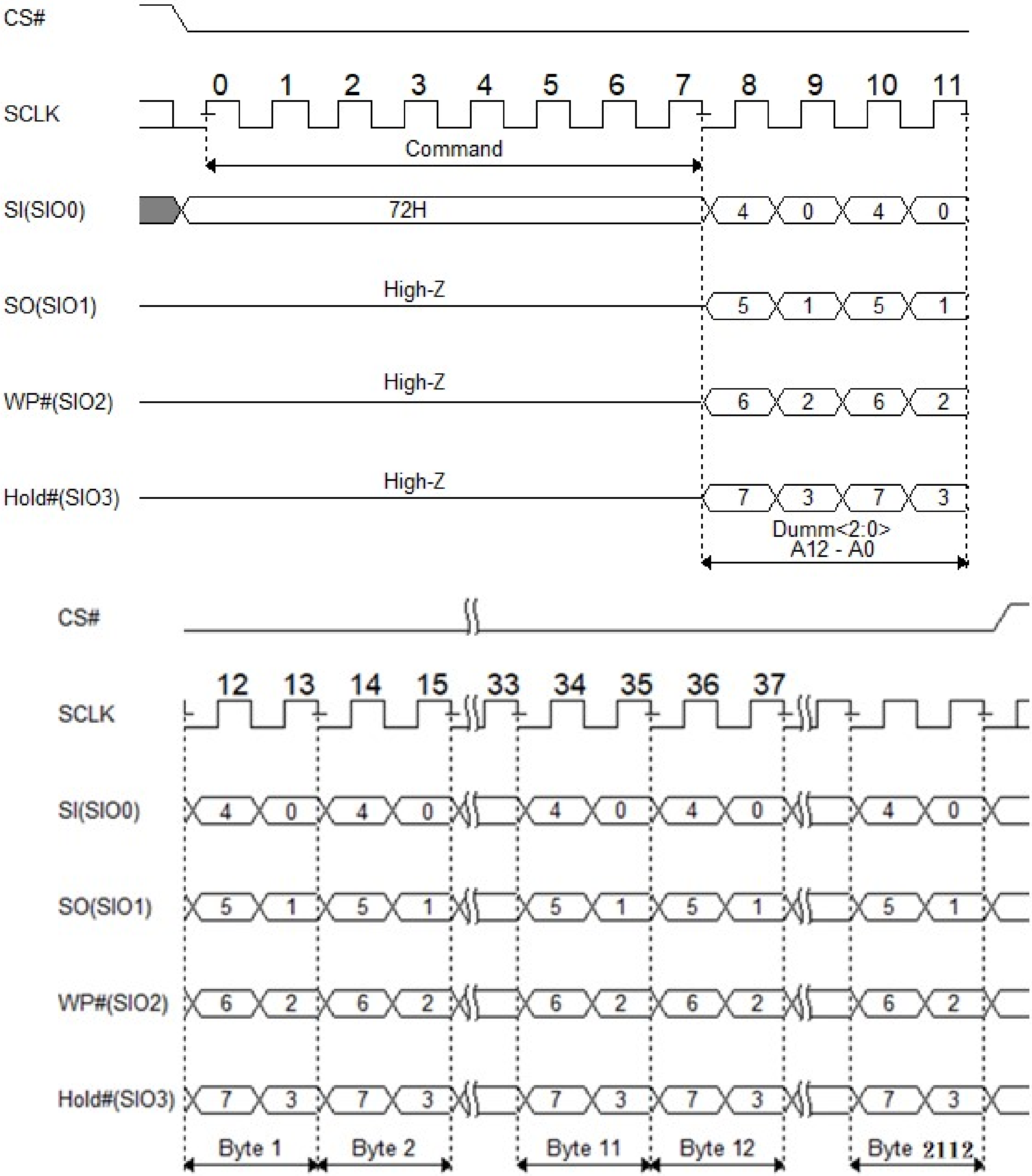
15.5. Program Load Random Data Move x4 (C4/34H)

Internal data move with 4x bus width.



15.6. Program Load Random Data Move Quad IO (72H)

Internal data move with 4x bus width and treat address field is 4x data width.



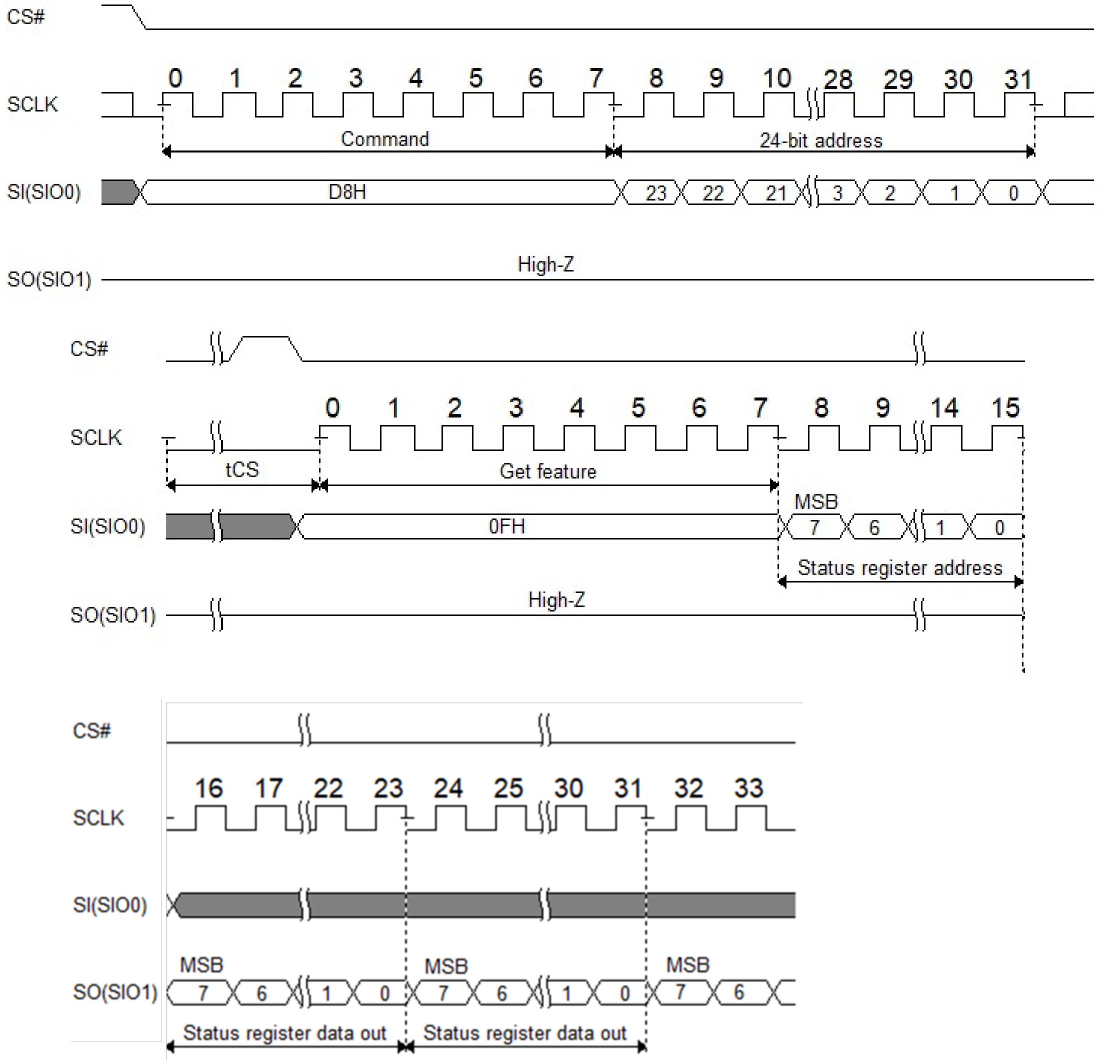
16. Block ERASE (D8H)

The Block Erase (D8H) command is used to erase at block level. The command sequence for BLOCK ERASE operation is as following

- 06H (WRITE ENABLE command)
- D8H (BLOCK ERASE command)
- 0FH (GET FEATURE command to read the status register)

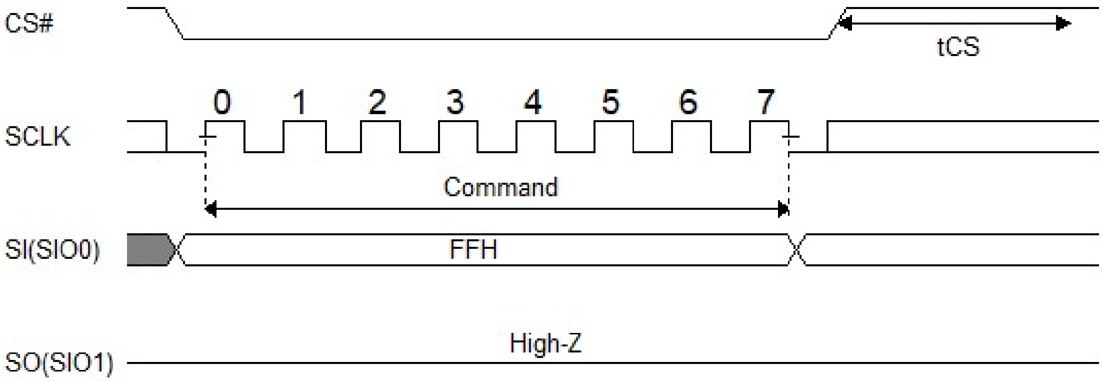
Erase Operation sequence starts from a WRITE ENABLE (06H) command to set WEL bit to 1. After executing the WRITE ENABLE command, BLOCK ERASE (D8H) command can be issued. BLOCK ERASE (D8H) requires a 24-bit address which consists of dummy bits and row address (page address in row address will be ignored automatically).

Issue the GET FEATURE (0FH) command to monitor the erase operation after issuing the BLOCK ERASE. The E_FAIL bit is status register can reflect whether the block erased successfully or not.



17. RESET (FFH)

The RESET (FFH) command stops all operation. If there is a previous operation is execute or pended in cache it will be stopped executing.



18. Advanced Feature

18.1. Internal ECC

DM SPI NAND Flash provides the internal ECC which can protect user data without other controlling sequence. ECC could use the spare area in NAND FLASH memory and the occupied size is determined by the +ECC protected abilities.

The ECC is enabled after device power up.

During a PROGRAM operation, the device calculates an ECC code on the 2k page in the cache register, before the page is written to the NAND Flash array.

With internal ECC, the user must accommodate the following:

- Spare area definitions provided in the ECC Protection table below.
- ECC can protect according main and spare areas. WRITEs to the ECC area are ignored.

ECC Protection and Spare Area (Ex: Page= 2KB + 64B)

Page Structure	Main Memory Array (2,048-Byte) Page Structure							
	Max Byte Address	**Min Byte Address**	**Area**		**Size**		**ECC Protected**	**Note**
2,112-Byte	1FFh	000h	Sector 0		512B		YES	
	3FFh	200h	Sector 1		512B		YES	
	5FFh	400h	Sector 2		512B		YES	
	7FFh	600h	Sector 3		512B		YES	
	Spare Area (64-Byte)							
	Max Byte Address	**Min Byte Address**	**Area**	**Byte Definition**	**Size**		**ECC Protected**	**Note**
	80Fh	800h	Spare 0	Bad Block Marker	16B	2B	NO	

				User Date II		2B	NO	
				User Date I		4B	YES	
				ECC for Spare 0		6B	YES	
				ECC for Spare		2B	YES	ECC for User Data I & ECC for Spare 0
	81Fh	810h	Spare 1	Bad Block Marker	16B	2B	NO	
				User Date II		2B	NO	
				User Date I		4B	YES	
				ECC for Spare 1		6B	YES	
				ECC for Spare		2B	YES	ECC for User Data I & ECC for Spare 1
	82Fh	820h	Spare 2	Bad Block Marker	16B	2B	NO	
				User Date II		2B	NO	
				User Date I		4B	YES	
				ECC for Spare 2		6B	YES	
				ECC for Spare		2B	YES	ECC for User Data I & ECC for Spare 2
	83Fh	830h	Spare 3	Bad Block Marker	16B	2B	NO	
				User Date II		2B	NO	
				User Date I		4B	YES	
				ECC for Spare 3		6B	YES	
				ECC for Spare		2B	YES	ECC for User Data I & ECC for Spare 3

18.2. Status Register

The device has an 8-bit status register that software can read during the device operation for operation state query. The status register can be read by issuing the GETFEATURES(0FH) command, followed by the feature address C0h (see Feature Operation)

Bit	Bit Name	Description
P_FAIL	Program Fail	This bit indicates that a program failure has occurred (P_FAIL set to 1). It will also be set if the user attempts to program an invalid address or a protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_FAIL = 0). This bit is only valid after a page programming command (0x10)
E_FAIL	Erase Fail	This bit indicates that an erase failure has occurred (E_FAIL set to 1). It will also be set if the user attempts to erase a locked region. This bit is cleared (E_FAIL = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
WEL	Write Enable Latch	This bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command.
OIP	Operation In Progress	This bit indicate thata PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, or RESET is in progress
ECCS2 ~ ECCS0	ECC Status	ECCS provides ECC status as follows: ECCSx is set to 0000b either following a RESET, or at the beginning of the READ. It is then updated after the device completes a valid READ operation. ECCS is invalid if internal ECC is disabled (via a SET FEATURES command to reset ECC_EN to 0). After power-on RESET, ECC status is set to reflect the contents of block 0, page 0.ECCS1/0 bits are only valid after a page read command (0x13)

Hereunder is the EXSAMPLE for ECC status

Example 1 : ECC Status (Page= 2KB + 64B)

ECCS2	ECCS1	ECCS0	Description
0	0	0	No bit errors.
0	0	1	Bit errors (<=3) were detected and corrected.
0	1	0	Bit errors (<=6) were detected and corrected.
0	1	1	Bit errors (<=9) were detected and corrected.
1	0	0	Bit errors (<=12) were detected and corrected.
1	0	1	Bit errors (<=15) were detected and corrected.
1	1	0	Bit errors (=16) were detected and corrected.
1	1	1	Bit errors>=17, error exceeded. And cannot be corrected.

Example 1 : ECC Status (Page= 2KB + 128B)

ECCS2	ECCS1	ECCS0	Description
0	0	0	No bit errors.
0	0	1	Bit errors (<=4) were detected and corrected.
0	1	0	Bit errors (<=8) were detected and corrected.
0	1	1	Bit errors (<=12) were detected and corrected.
1	0	0	Bit errors (<=16) were detected and corrected.
1	0	1	Bit errors (<=20) were detected and corrected.
1	1	0	Bit errors (<=24) were detected and corrected.
1	1	1	Bit errors>=25, error exceeded. And cannot be corrected.

18.3. Strength Register

DS_S1	DS_S0	Driver Strength
0	0	50%
0	1	25%
1	0	75%
1	1	100%

19. Electronic characteristic

19.1. Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-55°C ~ 125°C
Ambient Operation Temperature	-40°C ~ 85°C
Applied Input/Output Voltage	0V ~ VCC*1.1

19.2. DC Characteristics

Parameters	Min	Typical	Max	UNIT
Supply Voltage (VCC)	2.7	3.3	3.6	V
Input Leakage Current			2	uA
Output Leakage Current			2	uA
Operation Current (Read)		30	40	mA
Standby Current			70	uA

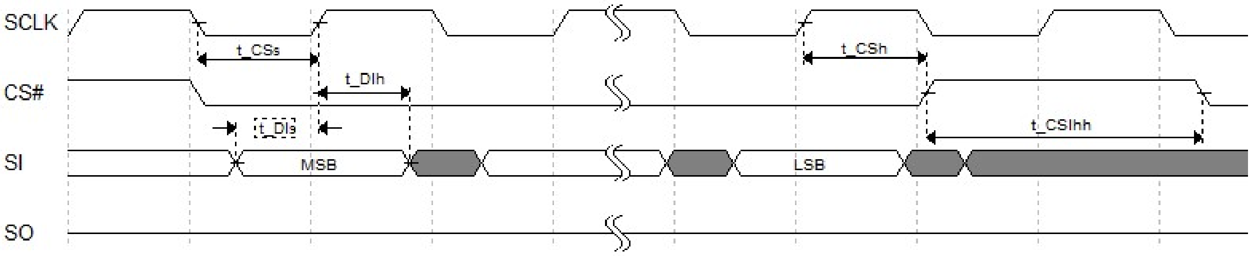
19.3. Program and Erase Timing

Parameters	Min	Typical	Max	UNIT
Next Command After Reset			510	us
Read from Array			82	us
Page Programing Time		0.4	0.7	ms
Block Erase Time		2.8	5.5	ms

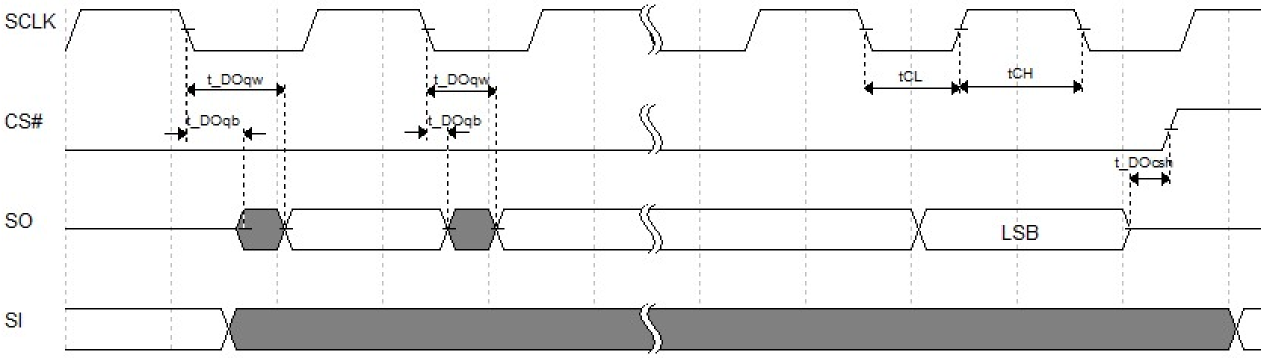
20. Timing characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit
Fop	Serial clock frequency			104	Mhz
t_CH	Clock high duty	4		4.8	ns
t_CL	Clock low duty	4		4.8	ns
t_CSs	CS# active setup time	2			ns
t_CSh	CS# active hold time	4			ns
t_DOs	DATA IN setup time	2			ns
t_DOh	DATA IN hold time	2			ns
t_CSlhh	The timing of CS# to keep from low to high	5			ns
t_DOqw	Max delay from clock to data output			8	ns
t_DOqb	Min delay from clock to data input	6			ns
t_DOcsh	DATA output disable timing			20	ns
t_CHhl	HOLD# Hold time in high	5			ns
t_CHhh	HOLD# Hold time in low	5			ns
t_HHch	HOLD# Setup time in high	5			ns
t_HLch	HOLD# Setup time in low	5			ns
t_HHqx	HOLD# Output from high to Low-z			15	ns
t_HLqz	HOLD# Output from high to High-z			15	ns

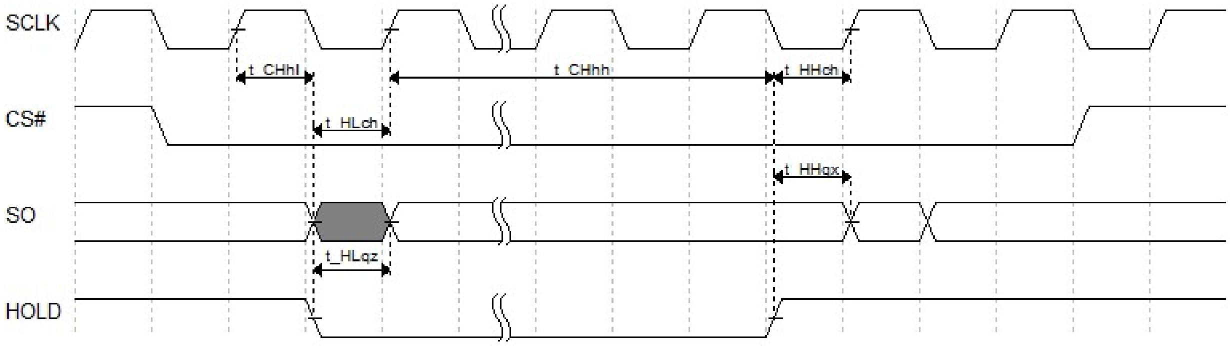
SPI input timing diagram



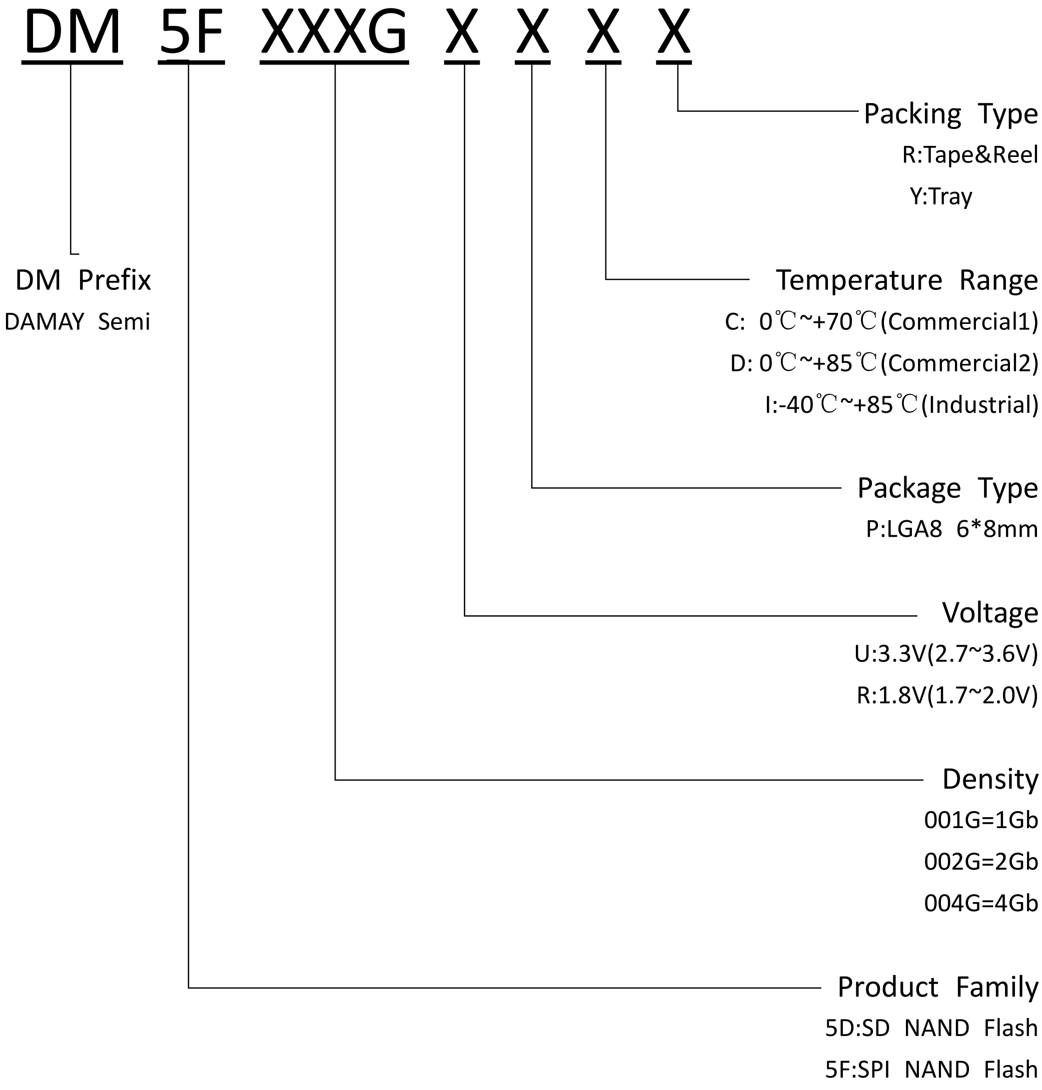
SPI output timing diagram



SPI HOLD timing diagram



21. Part Information



DM 5F XXXG X X X X

Packing Type
R:Tape&Reel
Y:Tray

DM Prefix
DAMAY Semi

Temperature Range
C: 0℃~+70℃(Commercial1)
D: 0℃~+85℃(Commercial2)
I:-40℃~+85℃(Industrial)

Package Type
P:LGA8 6*8mm

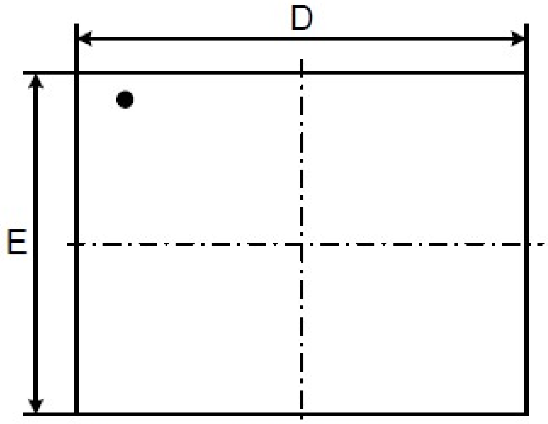
Voltage
U:3.3V(2.7~3.6V)
R:1.8V(1.7~2.0V)

Density
001G=1Gb
002G=2Gb
004G=4Gb

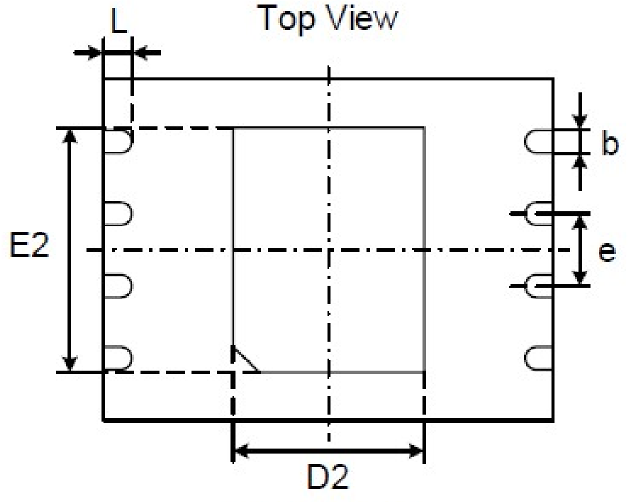
Product Family
5D:SD NAND Flash
5F:SPI NAND Flash

22. Package

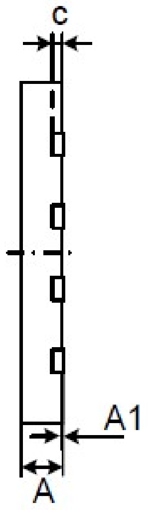
LGA8 (6mm*8mm)



Top View



Bottom View



Side View

Dimensions

Symbol Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.240	0.173		0.022