DM5DXXXGXXXX

SD-NAND FLASH

DATASHEET

Product List

Part Number	Flash Type	Capacity	Temperature	Package	Size
DM5D001GUPIY	SLC	1Gbit	-40^{O}C ~ 85^{O}C	LGA-8	6x8mm
DM5D002GUPIY	SLC	2Gbit	-40^{O}C ~ 85^{O}C	LGA-8	6x8mm
DM5D004GUPIY	SLC	4Gbit	-40^{O}C ~ 85^{O}C	LGA-8	6x8mm
DM5D032GUSCY	MLC	32Gbit	-40^{O}C ~ 85^{O}C	LGA-16	9x12.5mm

Rev1.10 2005

DM Damay semi

SHENZHEN DAMAY SEMICONDUCTOR COMPANY LIMITED

Table of Content

目录

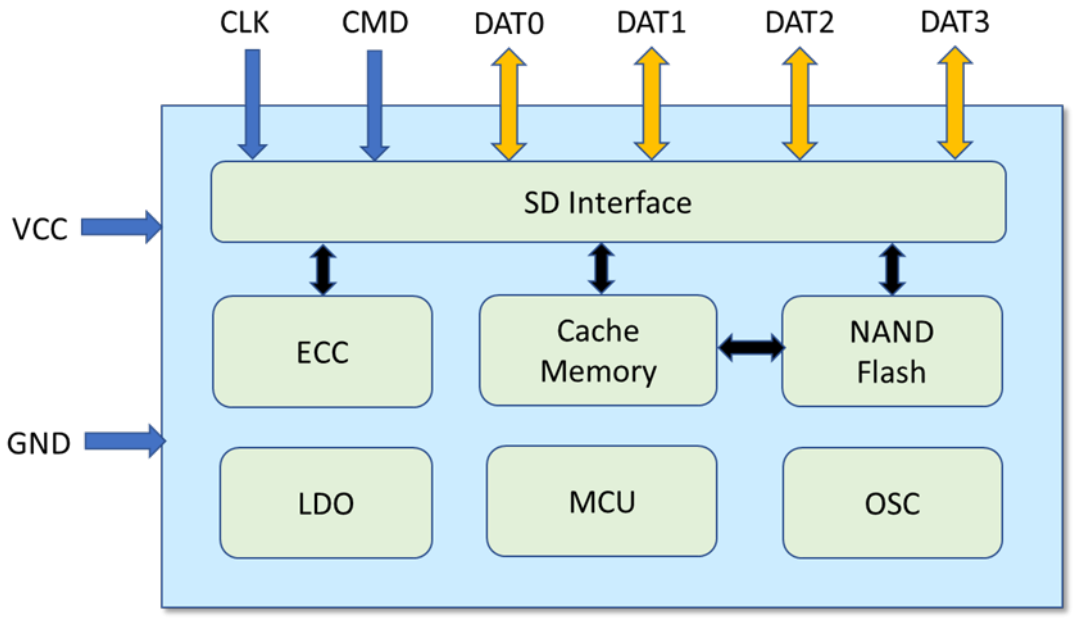
1. Description

SD NAND Flash is an embedded storage solution for low-power application. The SD NAND Flash is based on an advance 8-pin interface (clock, command, Data*4, power and ground). The SD NAND Flash is fully compliant with SD2.0/SD3.0 interface and operation is similar to SD card.

2. Features

- Advance
  - Advanced dynamic ECC engine to improve reliability
  - Support Data Randomizer
  - Support Program Fail Recovery
- SD2.0/3.0 Interface
  - Complies to SD specifications version 2.x/3.0x
  - Support UHS-I (SDR50, SDR104, DDR50)
  - Support clock frequencies 0~208MHz
- Enhanced access performance
  - 4KB cache for fast random read
  - Cache read and cache program
- Power Supply and Consumption
  - Voltage range: 2.7V ~ 3.6V
  - Active: 80mA (Typical)
  - Standby: 160uA (Typical)
- Temperature
  - Operation : Commercial1: $0^{O}C$ ~ $70^{O}C$
    Commercial2: $0^{O}C$ ~ $85^{O}C$
    Industrial:-$40^{O}C$ ~ $85^{O}C$
  - Storage: -$55^{O}C$ ~ $125^{O}C$

3. Block Architecture



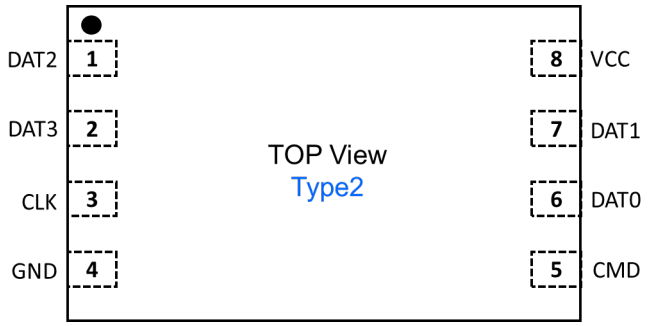
4. Product List

Part Number	Flash Type	Capacity	Temperature	Package	Size
DM5D001GUPIY	SLC	1Gbit	-40^{O}C ~ 85^{O}C	LGA-8	6x8mm
DM5D002GUPIY	SLC	2Gbit	-40^{O}C ~ 85^{O}C	LGA-8	6x8mm
DM5D004GUPIY	SLC	4Gbit	-40^{O}C ~ 85^{O}C	LGA-8	6x8mm
DM5D032GUSCY	MLC	32Gbit	-40^{O}C ~ 85^{O}C	LGA-16	9x12.5mm

5. Pin Description

5.1. WSON8/LGA8 6*8mm/6.6*8mm

Device Top View

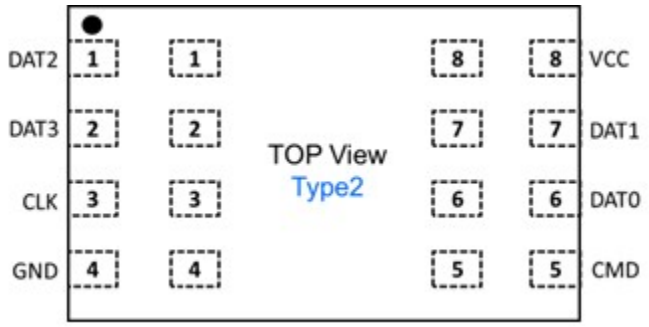


Pin Definition

Pin Name	IO type	Description
DAT3	In/Out	Data line (Bit 3)
DAT0	In/Out	Data line (Bit 0)
DAT1	In/Out	Data line (Bit 1)
GND	Ground	Ground
CMD	In/Out	Command
CLK	Input	SD clock
DAT2	In/Out	Data line (Bit 2)
VCC	Supply	Main supply power

5.2. LGA-16 9*12.5mm

Device Top View



Pin Definition

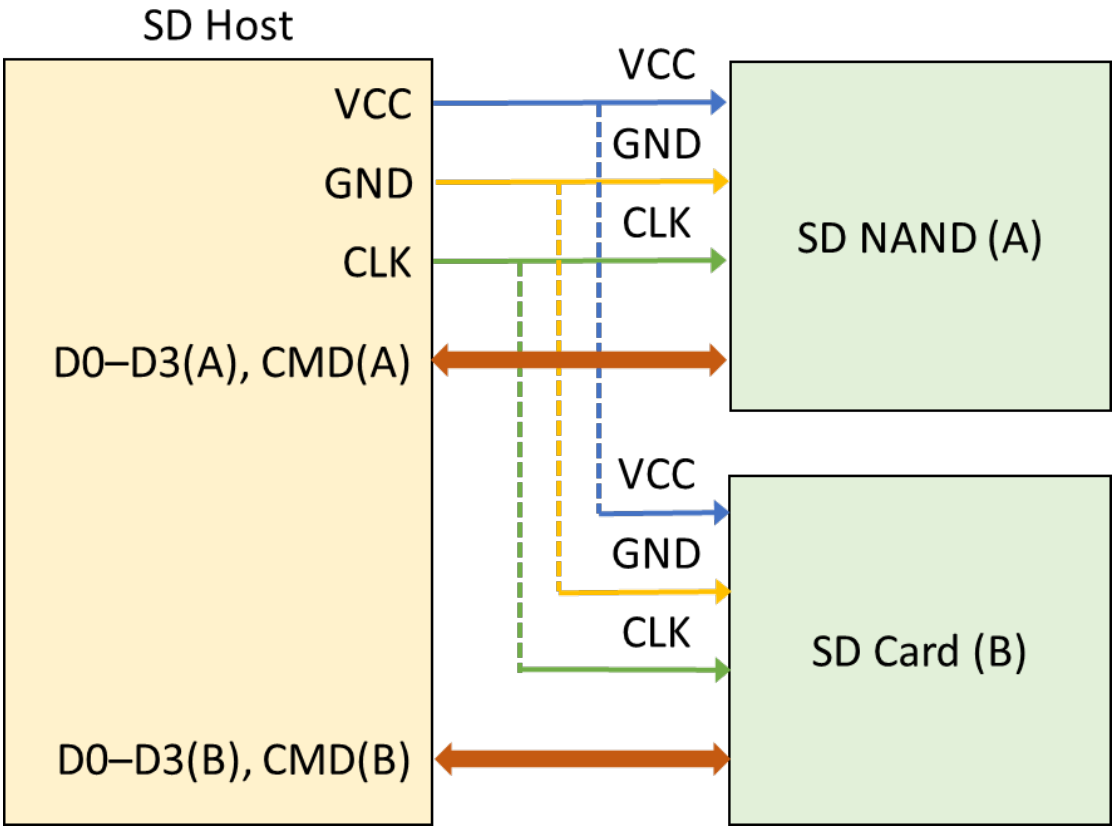
Pin Name	IO type	Description
DAT3	In/Out	Data line (Bit 3)
DAT0	In/Out	Data line (Bit 0)
DAT1	In/Out	Data line (Bit 1)
GND	Ground	Ground
CMD	In/Out	Command
CLK	Input	SD clock
DAT2	In/Out	Data line (Bit 2)
VCC	Supply	Main supply power

6. SD Bus Mode Protocol

The SD bus has six communication lines and three supply lines:

- CMD: Command is bi-directional signal.
- DAT0-3: Data lines are bi-directional signals.
- CLK: Host clock signal
- VCC: Power supply.
- GND: Ground

The following figure shows the bus topology with one host in SD Bus mode.



7. Function Description

The sector size of the SD NAND Flash is 512-byte which is the same as that in an IDE magnetic disk drive. To write or read a sectors, the host computer software simply issues a Read or Write command to the SD NAND Flash.

7.1. ECC

DM SD NAND Flash provides the internal ECC which can protect user data without other controlling sequence. ECC could use the spare area in NAND FLASH memory and the occupied size is determined by the +ECC protected abilities. The ECC default setting is enabled after device power up.

7.2. Bad Block Manage

The device occasionally contains bad blocks. Please read one word of first page of first spare in each block. SF makes sure that every invalid block has data at this word. If the data of the word is “0”, define the block as a bad block.

7.3. Automatic Sleep Mode

SD NAND Flash provides automatic entrance and exit from sleep mode. If no further commands are received within 5msec, chip would enter sleep mode. The host does not have to take any action for this to occur. SD NAND Flash provide ultra-low power consumption during sleep mode (around 70uA) and suitable for IoT application.

7.4. Wear Leveling

Wear-leveling is an intrinsic part of the Erase Pooling functionality of SD using NAND memory. The Wear Level command is supported as a NOP operation to maintain backward compatibility with existing software utilities.

8. Registers

Six registers are defined within the card interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters

Register	Width	Comment
OCR	32	Operation Conditions Register
CID	128	Card IDentification
CSD	128	Card-Specific Data
RCA	16	Relative Card Address
DSR	16	Driver Stage Register
SCR	64	SD CARD Configuration Register
SD Status	512	Status Bits and Card Features

8.1. OCR Register

The 32-bit operation conditions register stores the VDD voltage profile. Additionally, this register includes status information bits. One status bit is set if the power up procedure has been finished. This register includes another status bit indicating the capacity status after set power up status bit.

Bit Position	OCR Fields Definition	Bit Position	OCR Fields Definition
0-3	Reserved	16	2.8 ~ 2.9
4	Reserved	17	2.9 ~ 3.0
5	Reserved	18	3.0 ~ 3.1
6	Reserved	19	3.1 ~ 3.2
7	Reserved for low voltage range	20	3.2 ~ 3.3
8	Reserved	21	3.3 ~ 3.4
9	Reserved	22	3.4 ~ 3.5
10	Reserved	23	3.5 ~ 3.6
11	Reserved	24(1)	Switching to 1.8V Accepted (S18A)
12	Reserved	25-29	Reserved
13	Reserved	30	Card Capacity Status (CCS)(2)
14	Reserved	31	Card power up status bit (busy)(3)
15	2.7 ~ 2.8		

(1) Only UHS-I card supports this bit.

(2) This bit is valid only when the card power up status bit is set.

(3) This bit is set to LOW if the card has not finished the power up routine.

8.2. CID Register

The CID register is 16 bytes long and contains a unique identification number as shown in below table.

Name	Width	CID Slice	Comment
Manufacture ID (MID)	8	[127:120]	The manufacturer IDs are controlled and assigned by the SD Card Association.
OEM/Application ID (OID)	16	[119:104]	Identifies the card OEM and/or the card contents. The OID is assigned by the 3C.*
Product Name (PNM)	40	[103: 64]	5 ASCII characters long
Product Revision (PRV)	8	[63:56]	Two binary coded decimal digits
Serial Number (PSN)	32	[55:24]	32 Bits unsigned integer
Reserved	4	[23:20]	
Manufacture Data Code (MDT)	12	[19:8]	Manufacture date–yym (offset from 2000)
CRC7 checksum (CRC)	7	[7:1]	Calculated
Not used, always 1	1	[0:0]	

8.3. CSD Register

The Card-Specific Data register provides information regarding access to the device contents. The CSD defines the data format, error correction type, maximum data access time, whether the DSR register can be used, etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The types of the entries in the table below are coded as follows: R = readable, W(1) = writable once, W = multiple writable.

Field	Width	Value	Type	CSD-slice
CSD_STRUCTURE	2	00b	R	[127:126]
-	6	00 0000b	R	[125:120]
TAAC	8	xxh	R	[119:112]
NSAC	8	xxh	R	[111:104]
TRAN_SPEED	8	32h or 5Ah	R	[103:96]
CCC	12	01x110110101b	R	[95:84]
READ_BL_LEN	4	xh	R	[83:80]
READ_BL_PARTIAL	1	1b	R	[79:79]
WRITE_BLK_MISALIGN	1	xb	R	[78:78]
READ_BLK_MISALIGN	1	xb	R	[77:77]
DSR_IMP	1	xb	R	[76:76]
-	2	00b	R	[75:74]
C_SIZE	12	xxxh	R	[73:62]
VDD_R_CURR_MIN	3	xxxb	R	[61:59]
VDD_R_CURR_MAX	3	xxxb	R	[58:56]
VDD_W_CURR_MIN	3	xxxb	R	[55:53]
VDD_W_CURR_MAX	3	xxxb	R	[52:50]
C_SIZE_MULT	3	xxxb	R	[49:47]
ERASE_BLK_EN	1	xb	R	[46:46]
SECTOR_SIZE	7	xxxxxxxb	R	[45:39]
WP_GRP_SIZE	7	xxxxxxxb	R	[38:32]
WP_GRP_ENABLE	1	xb	R	[31:31]
-	2	00b	R	[30:29]
R2W_FACTOR	3	xxxb	R	[28:26]
WRITE_BL_LEN	4	xxxxb	R	[25:22]
WRITE_BL_PARTIAL	1	xb	R	[21:21]

Field	Width	Value	Type	CSD-slice
-	5	00000b	R	[20:16]
FILE_FORMAT_GRP	1	xb	R/W(1)	[15:15]
COPY	1	xb	R/W(1)	[14:14]
PERM_WRITE_PROTECT	1	xb	R/W(1)	[13:13]
TMP_WRITE_PROTECT	1	xb	R/W	[12:12]
FILE_FORMAT	2	xxb	R/W(1)	[11:10]
-	2	00b	R/W	[9:8]
CRC	7	xxxxxxxb	R/W	[7:1]
-	1	1b	-	[0:0]

8.4. RCA Register

The writable 16-bit relative card address register carries the device address that is published by the device during the identification. This address is used for the addressed host-device communication after the identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7

8.5. DSR Register

The 16-bit driver stage register is described in detail in Chapter 6.5. It can be optionally used to improve the bus performance for extended operating conditions (depending on parameters like bus length, transfer rate or number of devices). The CSD register carries the information about the DSR register usage. The default value of the DSR register is 0x404.

8.6. SCR Register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the SD Memory Device's special features that were configured into the given device. The size of SCR register is 64 bits. This register shall be set in the factory by the SD Memory Device manufacturer. The following table describes the SCR register content

Field	Width	Type	CSD-slice
SCR_STRUCTURE	4	R	[63:60]
SD_SPEC	4	R	[59:56]
DATA_STAT_AFTER_ERASE	1	R	[55:55]
SD_SECURITY	3	R	[54:52]
SD_BUS_WIDTHS	4	R	[51:48]
SD_SPEC3	1	R	[47]
-	13		[46:34]
CMD_SUPPORT	14	R	[33:32]
-	32	R	[31:0]

9. Electronic characteristic

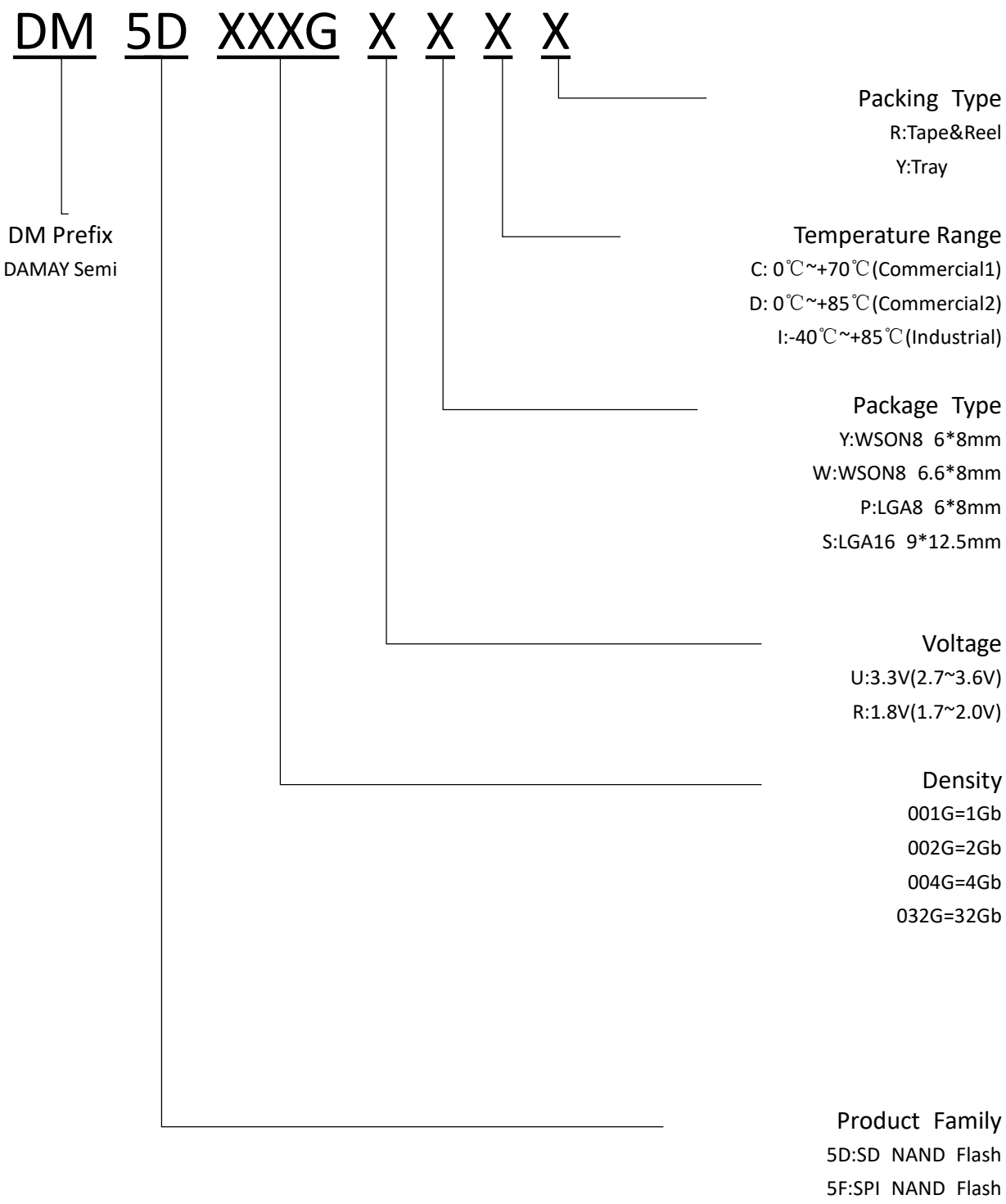
9.1. Absolute Maximum Ratings

Parameter	Value
Storage Temperature	-55^{O}C ~ 125^{O}C
Ambient Operation Temperature	-0^{O}C ~ 70^{O}C
Applied Input/Output Voltage	0V ~ VCC*1.1

9.2. DC Characteristics

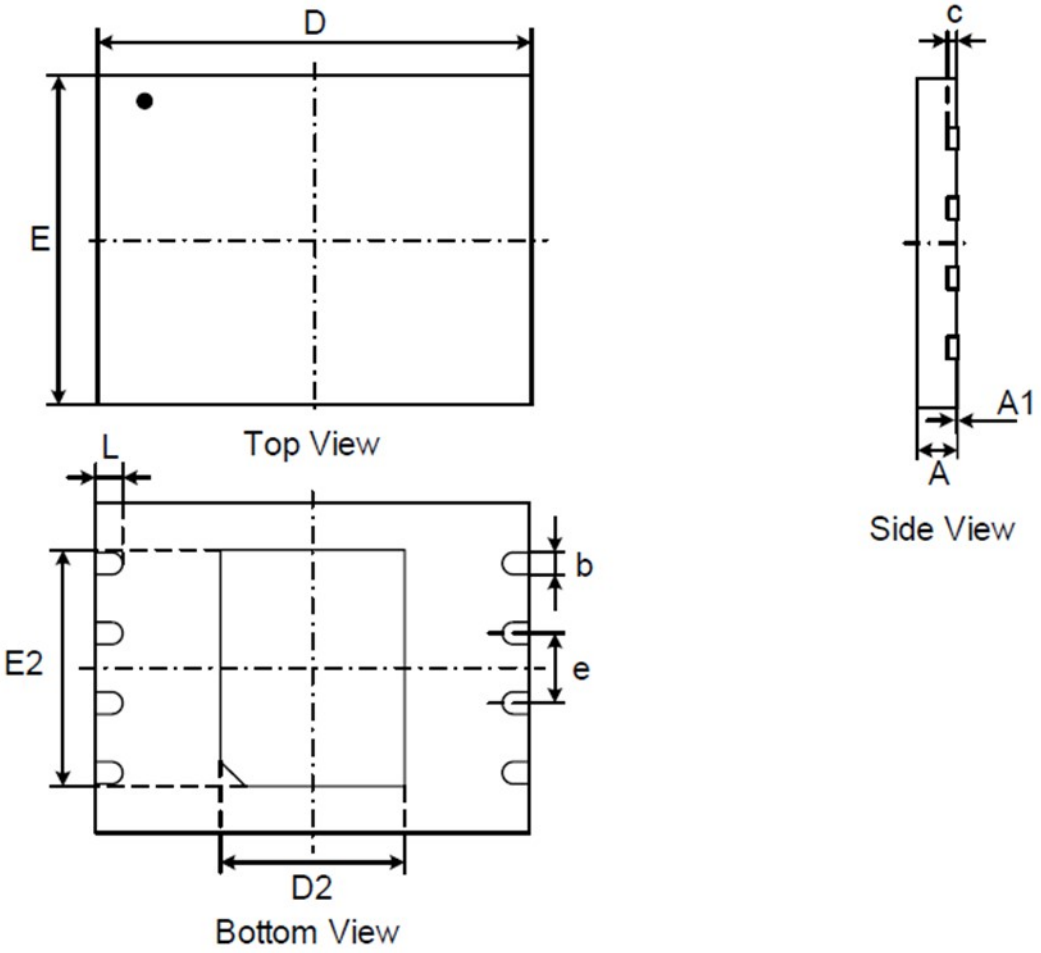
Parameters	Min	Typical	Max	UNIT
Supply Voltage (VCC)	2.7	3.3	3.6	V
Input Leakage Current	---	---	5	uA
Output Leakage Current	---	---	5	uA
Operation Current (Read)	---	80	---	mA
Operation Current (Write)	---	40	---	mA
Standby Current	---	160	---	uA

10. Part Information



11. Package

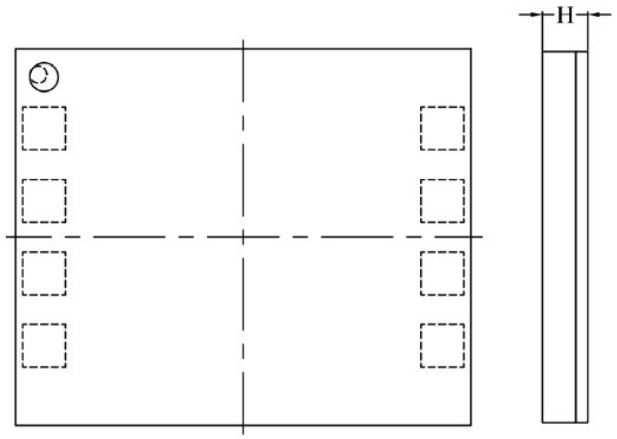
LGA8 /WSON8 (6mm*8mm)

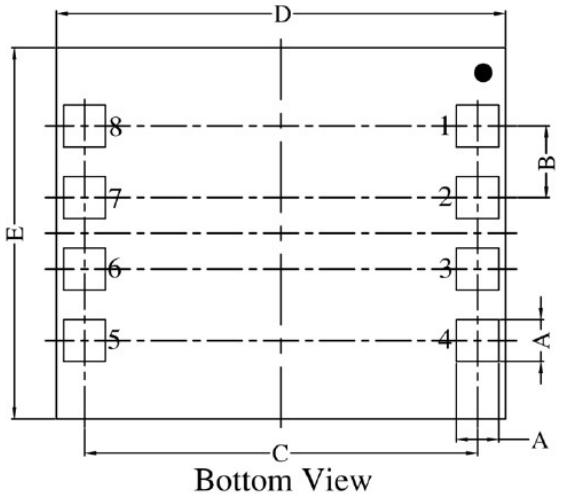


Dimensions

Symbol / Unit		A	A1	c	b	D	D2	E	E2	e	L
mm	Min	0.70	0.00	0.180	0.35	7.90	3.30	5.90	4.20	1.27	0.45
	Nom	0.75	0.02	0.203	0.40	8.00	3.40	6.00	4.30		0.50
	Max	0.80	0.05	0.250	0.45	8.10	3.50	6.10	4.40		0.55
Inch	Min	0.028	0	0.007	0.014	0.311	0.130	0.232	0.165	0.05	0.018
	Nom	0.030	0.001	0.008	0.016	0.315	0.134	0.236	0.169		0.020
	Max	0.032	0.002	0.010	0.018	0.319	0.138	0.240	0.173		0.022

WSON8 (6.6mm*8mm)

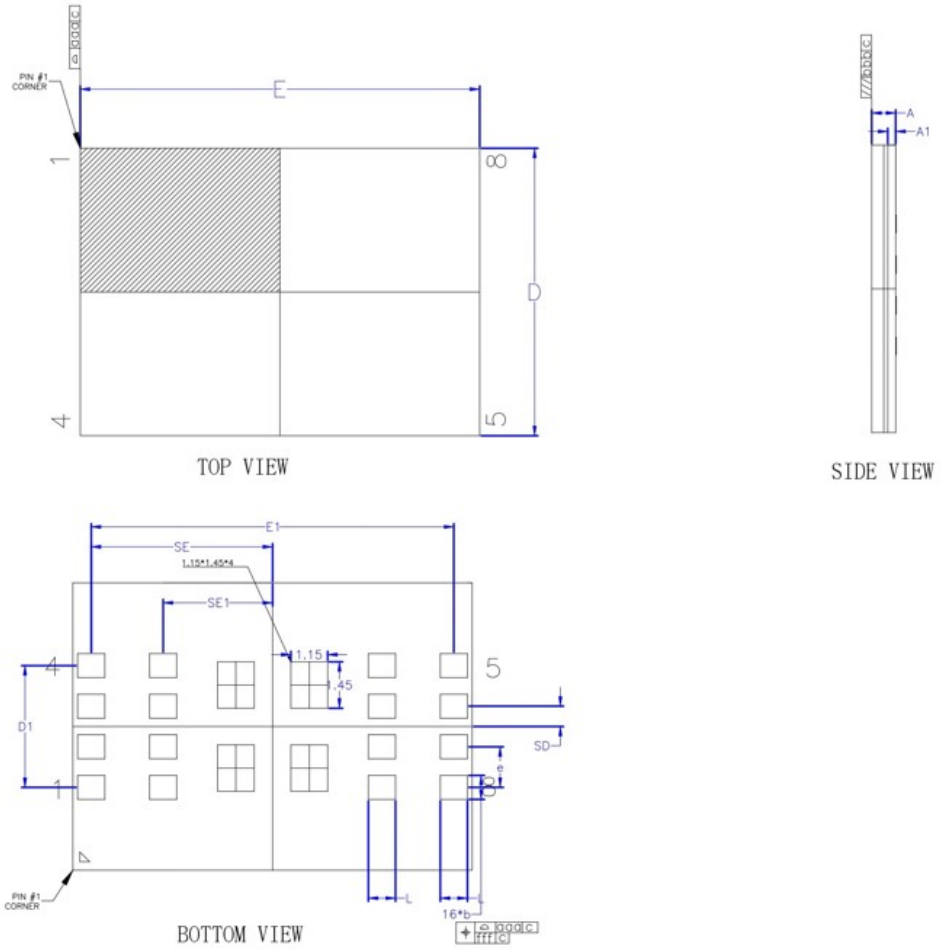




Pin Number	Name
1	SDD2
2	SDD3
3	SCLK
4	VSS
5	CMD
6	SDD0
7	SDD1
8	VCC

Common Dimensions (mm)				
Symbol	Min	Nom	Max	Note
A	0.65	0.75	0.85	
B	1.17	1.27	1.37	
C	6.90	7.00	7.10	
D	7.90	8.00	8.10	
E	6.50	6.60	6.70	
H	0.75	0.85	0.95	

LGA16 (9mm*12.5mm)



Dimensions

Item	D	E	D1	E1	A	A1	aaa	bbb	eee	fff	SE	SE1	SD	e	L	b
Unit	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm	mm
Spec	9.10 (9.00) 8.90	12.60 (12.50) 12.40	3.91 (3.81) 3.71	11.45 (11.35) 11.25	0.80 (0.75) 0.70	0.27 (0.25) 0.23	0.10	0.10	0.15	0.05	5.67BSC	3.425BSC	0.635BSC	1.27BSC	0.90 0.85 0.80	0.80 0.75 0.70